Multilevel Voltage Space Phasor Generation for an Open-end Winding Induction Motor Drive

K.C. Sekhar, *Member, IEEE* and G.T. Ram Das, *Member, IEEE*

Abstract — **A topology for multilevel voltage space phasor generation for an open-end winding induction motor drive is presented in this paper. The open-end winding induction motor is fed from both ends by two 3-level inverters. Each 3-level inverter is formed by cascading two 2-level inverters. This results in voltage space phasor levels equivalent to a conventional 8-level inverter. The proposed 8-level inverter configuration requires lesser number of switching devices as compared to conventional 8-level inverter scheme. Compared to the H-bridge topology, the proposed scheme uses a lower number of power supplies. In the multilevel carrier-based Sinusoidal Pulse Width Modulation (SPWM), used for the proposed drive, a progressive discrete DC bias depending on the speed range is given to the reference wave so that the drive can operate in the i-level modes (i=2, 3, …8) depending on the speed range. The inverter with the higher DC-link voltage is switching less frequently, compared to the inverter with the lower DC-link voltage.**

Index Terms — **Multilevel inversion, open-end winding Induction motor drive**

I. INTRODUCTION

Multilevel converters have found increased relevance in the area of high power high voltage applications. The high power drive systems fed from multi-level inverters of higher levels, with lesser power circuit complexity and costs, are the centre of attraction from the industrial sector. Different multilevel topologies are proposed and studied extensively for drive applications as well as utility applications [1]–[9]. As the number of levels increases, the output waveform has more steps of smaller voltage resulting in a more regular (near to sinusoidal) waveform. This result in the output voltage with less harmonic distortion [4] and thus the operating frequencies can be reduced for multilevel inverters as compared to 2-level inverters. In a multilevel topology, the switching devices are switched at reduced voltage, resulting in reduced *dv/dt* [4]. The multilevel inverters can be grouped into four main groups: Diode clamped or neutral point clamped inverter configurations, H-bridge cascaded configurations, flying capacitor topologies and multilevel inverter configurations obtained with feeding induction motor from both sides [5]–[9]. The open-end winding induction motor fed from both sides by two 3-level inverters, with symmetrical DC links, generates the voltage space vectors similar to conventional NPC 5-level inverter [7].

Higher-level voltage waveforms can be synthesized if the individual inverters are supplied with unequal DC link voltages [10] – [12]. The 7-level inverter scheme, using asymmetric DC link voltages, presented in [9] – [14], requires six isolated power supplies. A multilevel system that is capable of realizing a PWM waveform ranging from 2-level to 8-level is described in [15], which requires only four isolated power supplies. The scheme [15]

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uses an open-end winding induction motor, supplied by two 3-level inverters. Each 3-level inverter is a cascaded combination of two 2-level inverters [8]. The waveforms in [15] were obtained by switching the appropriate space vector combination using the look-up table. It is a formidable and cumbersome proposition to switch appropriate space vector combinations using look-up table approach.

In the present work, a multilevel carrier based PWM is implemented for the inverter system proposed in [15] where a progressive discrete DC-bias is given to the reference wave depending upon the speed range and this results in reduced inverter switchings. The inverter with the higher DC-link voltage is switching less frequently compared to the inverter with lower DC-link voltage. This multilevel carrier based PWM eliminates the use of look-up approach to switch the appropriate space vector combination as in [15].

II. PROPOSED POWER CIRCUIT CONFIGURATION

The structure of the proposed drive for open-end winding induction motor is shown in Fig.1. In this circuit configuration, an open-end winding induction motor is fed by two 3-level inverters, ' inverter A' and 'inverter B' from both ends. The 3-level inverters are realized by cascading two 2-level inverters. The 'inverter A' is formed by cascading 2-level inverters 'inverter-1' & 'inverter-2'. These 2-level inverters have separate DC supplies of $(3/7)V_{dc}$, and $(2/7)V_{dc.}$ The 'inverter B' is formed by cascading 2-level inverters 'inverter-3' & 'inverter-4' each having separate DC supply $(1/7)V_{dc.}$ Where V_{dc} is the DC-link voltage of an equivalent conventional single 2-level inverter drive.

For 'inverter A', let V_{A2o}, V_{B2o} and V_{C2o} represent pole voltages of A, B and C phases respectively, referred to the point 'O' (Fig.1). The two switches forming each leg of the 2-level inverters 'inverter-1' (referred as top inverter of 'inverter A') and 'inverter-2 (referred as bottom inverter) are switched in complementary manner. The pole voltages V_{A2o}, V_{B2o} and V_{C2o} of 'inverter A' can realize three levels 0, $(2/7)V_{dc}$ and $(5/7)V_{dc}$. When S_{24} is turned on, the A-phase pole voltage V_{A2o} becomes zero as the point A2 is connected to 'O'. Pole voltage on A-phase leg could reach a level of $(5/7)V_{dc}$ when S_{11} and S_{21} are turned on and pole voltage attains $(2/7)V_{dc}$ when S_{14} and S_{21} are turned on. Inverter-B is also a 3-level inverter of the same topology as 'Inverter A', realize by cascading the 2-level inverters 'inverter-3' and 'inverter-4'. Its pole voltages with respect to the point 'O'' viz, V_{A4o}, V_{B4o} and V_{C4o} can independently realize three levels of 0, $(1/7)V_{dc}$ and $(2/7)V_{dc}$, when similar switching as in the case of 'inverter A' is used. When these two 3-level inverters drive the induction motor from both sides each phase of the induction motor can attain eight different levels. To find the equivalent levels when 'inverter A' and 'inverter B' are switched independently, the point 'O' and 'O'' are assumed to be connected. The different levels, generated for A-phase when 'inverter A' and 'inverter B' are switched with different pole voltage levels are shown in Table-I.

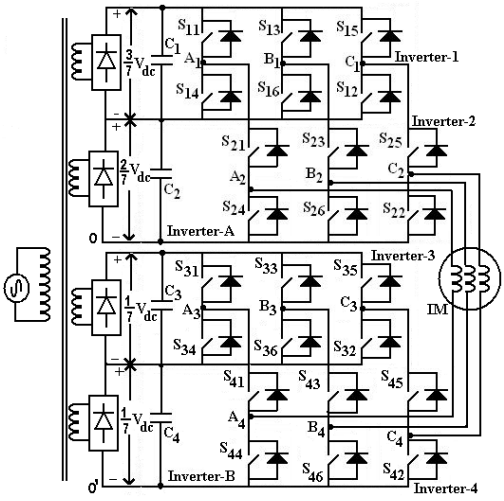

Fig. 1. Schematic circuit diagram of the proposed inverter drive scheme

It can be verified that all the other phases also can realize these eight levels. It can be seen that the first levels $-(2/7)V_{dc}$, $-(1/7)V_{dc}$ and 0 (L1, L2, L3) are obtained when 'inverter A' is clamped to zero while 'inverter B' is switched to $(2/7)V_{dc}$, $(1/7)V_{dc}$ and 0. For the fourth and fifth levels (L4, L5) 'inverter A' is clamped to its second level $(2/7)V_{dc}$, while

'inverter B' is switched to $(1/7)V_{dc}$ and 0. For the sixth, seventh and eighth levels 'inverter A' can be clamped to its third level $(5/7)V_{dc}$ while 'inverter B' to $(2/7)V_{dc}$, $(1/7)V_{dc}$ and 0. Hence the 'inverter A' is switched less frequently as the inverter operates in all these levels.

TABLE I
THE LEVELS REALIZED IN THE A-PHASE WINDING WHEN 'INVERTER A' AND 'INVERTER B' ARE SWITCHED INDEPENDENTLY

Pole-voltage of Inverter A (v_{A2O})	Pole-voltage of Inverter B ($v_{A4O'}$)	Motor phase voltage $v_{A2A4} = v_{A2O} - v_{A4O'}$	Level
0	$(2/7)\ V_{dc}$	$-(2/7)\ V_{dc}$	L1
0	$(1/7)\ V_{dc}$	$-(1/7)\ V_{dc}$	L2
0	0	0	L3
$(2/7)\ V_{dc}$	$(1/7)\ V_{dc}$	$(1/7)\ V_{dc}$	L4
$(2/7)\ V_{dc}$	0	$(2/7)\ V_{dc}$	L5
$(5/7)\ V_{dc}$	$(2/7)\ V_{dc}$	$(3/7)\ V_{dc}$	L6
$(5/7)\ V_{dc}$	$(1/7)\ V_{dc}$	$(4/7)\ V_{dc}$	L7
$(5/7)\ V_{dc}$	0	$(5/7)\ V_{dc}$	L8

It may be noted that when the bottom switch in a leg of the bottom inverters (inverter-2 or inverter-4) is ON, taking the machine winding end to O or O', the top switch of top inverter in the same leg could be ON or OFF. But if the top switch of the top inverter (inverter-1or inverter-4) is also made ON, the top switch of the bottom inverter would have to block twice DC link voltage [i.e. $(5/7)V_{dc}$ for 'inverter A' , $(2/7)V_{dc}$ for ' inverter B']. So whenever the bottom switch in any leg of the bottom inverter is ON, the top switch in the same leg of the top inverter is kept OFF.

The condition to be forced on the top switches of the inverters to realize these 8-levels in the A-phase is shown in the Table-II. The state of the bottom switch is complementary to the condition of the top switch in the same leg. The bottom switches of the bottom inverter of 'inverter A' (inverter-2) have to be rated for $(5/7)V_{dc}$, as they will have to block $(5/7)V_{dc}$ when the top switches of inverter-1 and inverter-2 are switched on. The bottom switches of the bottom inverter of 'inverter B' (inverter-4), have to be rated for $(2/7)V_{dc}$, as they will have to block $(2/7)V_{dc}$, when the top switches of 'inverter-3' are switched ON.

TABLE II
THE STATUS OF THE SWITCHES IN THE INVERTERS FOR EACH OF EIGHT LEVELS

Level in A-phase		Status of the top switches of the 2-level inverters (The bottom switches condition is complementary)			
	Voltage	Inver-1 S_{11}	Inver-2 S_{21}	Inver-3 S_{31}	Inver-4 S_{41}
L1	$-(2/7)V_{dc}$	OFF	OFF	ON	ON
L2	$-(1/7)V_{dc}$	OFF	OFF	OFF	ON
L3	0	OFF	OFF	OFF	OFF
L4	$(1/7)V_{dc}$	OFF	ON	OFF	ON
L5	$(2/7)V_{dc}$	OFF	ON	OFF	OFF
L6	$(3/7)V_{dc}$	ON	ON	ON	ON
L7	$(4/7)V_{dc}$	ON	ON	OFF	ON
L8	$(5/7)V_{dc}$	ON	ON	OFF	OFF

This 8-level topology does not need the clamping diodes as in the case of neutral-point clamped inverters. The DC-link capacitors do not carry the load current and hence the neutral-point fluctuations are absent. When compared with the series-connected H-bridge, it uses the less number of switching devices and DC-sources. The 7-level inverter configuration has further been improvised to yield an 8-level operation would results in a better waveform with lower THD.

III. VOLTAGE SPACE PHASORS OF PROPOSED SCHEME

The combined effect of three voltages in the three 120 degree separated phase winding of the induction motor at any instant, could be represented by an equivalent vector in space. This space vector V_s, for the dual inverter scheme is given by

$$V_s = V_{A2A4} + V_{B2B4} \cdot e^{j(2\pi/3)} + V_{C2C4} \cdot e^{j(4\pi/3)}. \quad (1)$$

Substituting expressions for the phase voltages in the above equation gives

$$V_s = (V_{A2O} - V_{A4O'}) + (V_{B2O} - V_{B4O'}). e^{j(2\pi/3)} + (V_{C2O} - V_{C4O'}). e^{j(4\pi/3)} \quad (2)$$

This equivalent vector can be determined by resolving the phase voltages along two mutually perpendicular axes, α-β axes of which α is along the A-phase(Fig.2). The space vector is then given by

$$V_s = V_s(\alpha) + jV_s(\beta) \quad (3)$$

Where V_s (α) is the sum of all components of V_{A2A4}, V_{B2B4} and V_{C2C4} along the 'α' axis and V_s (β) is the sum of the components V_{A2A4}, V_{B2B4} and V_{C2C4} along the 'β' axis. The voltage components Vs (α) and V_s (β) can be thus obtained by the following transformation

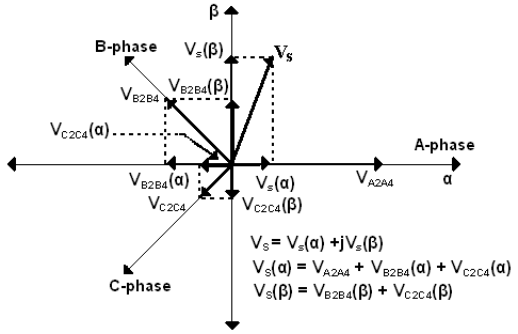

Fig. 2. Determination of equivalent space vector from phase voltages

$$V_S(\alpha) = V_{A2A4} + V_{B2B4}(\alpha) + V_{C2C4}(\alpha) \quad (4)$$

$$V_S(\beta) = V_{B2B4}(\beta) + V_{C2C4}(\beta) \quad (5)$$

$$\begin{bmatrix} V_S(\alpha) \\ V_S(\beta) \end{bmatrix} = \begin{bmatrix} 1 & -\frac{1}{2} & -\frac{1}{2} \\ 0 & \frac{\sqrt{3}}{2} & -\frac{\sqrt{3}}{2} \end{bmatrix} \begin{bmatrix} V_{A2A4} \\ V_{B2B4} \\ V_{C2C4} \end{bmatrix} \quad (6)$$

Substituting expressions for the phase voltages in the above equation gives

$$\begin{bmatrix} V_S(\alpha) \\ V_S(\beta) \end{bmatrix} = \begin{bmatrix} 1 & -\frac{1}{2} & -\frac{1}{2} \\ 0 & \frac{\sqrt{3}}{2} & -\frac{\sqrt{3}}{2} \end{bmatrix} \begin{bmatrix} V_{A2O} - V_{A4O'} \\ V_{B2O} - V_{B4O'} \\ V_{C2O} - V_{C4O'} \end{bmatrix} \quad (7)$$

The inverters can take different levels of pole voltages independently in the three phases depending upon the condition of the inverter switches and for each of the different combination of their pole voltages, V_{A2o}, V_{B2o} and V_{C2o} for the ' inverter A' and $V_{A4o'}$, $V_{B4o'}$ and $V_{C4o'}$ for the 'inverter B'. The equivalent voltage space phasor V_S, can be determined using equations (3) and (7). All the space phasors can be determined for all the possible combinations of the pole voltages of the two inverters. They will occupy different locations as shown in Fig.3, where the location marked '1' is the location of the zero amplitude space vector. There are in total 169 locations forming 294 sectors in the space vector point of view. The maximum amplitude of the space phasor generated can be verified to be V_{dc}.

A. Effect of Common-Mode Voltage in SpacePhasor Locations

In the above analysis for deriving the different levels and the space phasor locations, the points O and O' were assumed to be connected. When these points are not connected (as in the proposed drive Fig.1), the actual phase voltages are

$$V_{A2A4} = V_{A2O} - V_{A4O'} - V_{O'O} \quad (8)$$

$$V_{B2B4} = V_{B2O} - V_{B4O'} - V_{O'O} \quad (9)$$

$$V_{C2C4} = V_{C2O} - V_{C4O'} - V_{O'O} \quad (10)$$

$V_{O'O}$ corresponds to the common-mode voltage present in this balanced three-phase system and is given by

$$V_{O'O} = \tfrac{1}{3}(V_{A2O} + V_{B2O} + V_{C2O}) - \tfrac{1}{3}(V_{A4O'} + V_{B4O'} + V_{C4O'}) \quad (11)$$

Substituting these expressions for the phase voltages in (1)

$$V_S = (V_{A2O} - V_{A4O'} - V_{O'O}) + (V_{B2O} - V_{B4O'} - V_{O'O}).\, e^{j(2\pi/3)} + (V_{C2O} - V_{C4O'} - V_{O'O}).\, e^{j(4\pi/3)}$$

$$= (V_{A2O} - V_{A4O'}) + (V_{B2O} - V_{B4O'}).\, e^{j(2\pi/3)}$$

$$+ (V_{C2O} - V_{C4O'}).\ e^{j(4\pi/3)}$$

$$- (V_{O'O} + V_{O'O}.\ e^{j(2\pi/3)} + V_{O'O}.\ e^{j(4\pi/3)}) \quad (12)$$

In this equation

$$(V_{O'O} + V_{O'O}.\ e^{j(2\pi/3)} + V_{O'O}.\ e^{j(4\pi/3)})$$

$$= V_{O'O} - \tfrac{1}{2}\, V_{O'O} - \tfrac{1}{2}\, V_{O'O} = 0 \quad (13)$$

and the equation then reduces to

$$V_s = (V_{A2O} - V_{A4O'}) + (V_{B2O} - V_{B4O'}).\ e^{j(2\pi/3)} + (V_{C2O} - V_{C4O'}).\ e^{j(4\pi/3)} \quad (14)$$

This equation is the same as that derived earlier (2), assuming that points O and O' were connected. Hence the above analysis shows that the common-mode present between points O and O' does not change the space phasor locations. This common-mode voltage will result only in the multiplicity of space phasors in different locations, and the system with isolated O and O' points generates the same voltage-space phasors.

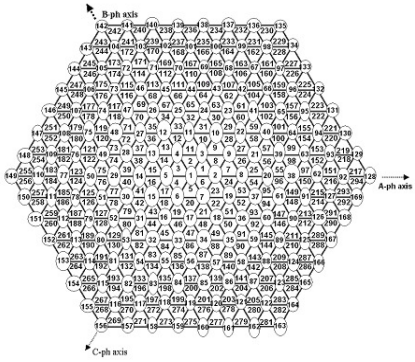

Fig. 3. The voltage space phasor locations for the proposed drive 169 locations forming 294 triangular sections equivalent to a 8-level Inverter.

IV. MODULATION SCHEME FOR THE PROPOSED INVERTER

Multilevel carrier based SPWM is used for the proposed inverter scheme. The multilevel carrier based PWM for an N-level inverter uses a set of N-1 adjacent level shifted triangular carrier waves with the amplitude and frequency If reference wave has peak amplitude V_m^* and frequency f_m, the modulation index is defined with reference to a triangular wave of peak-to –peak amplitude of V_C (N-1) as

$$M_a = 2V_m^* / V_C\ (N\text{-}1). \quad (15)$$

For the 8-level inverter drive structure, 7 triangular waves C1 to C7, with peak-to-peak amplitude of V_C are used, as shown in Fig.4(a). The peak-to-peak amplitude of each carrier is $V_C = (1/7)V_{max}$, where V_{max} is the maximum value possible for the modulating signal. These seven carriers divide the entire range of modulating signal to eight regions R1 to R8, R1 being the region below the lowest carrier C1 and R8 the region above the highest carrier C7. The regions between these two carriers are referred as R2 to R7. When the modulating signal is in a particular region a corresponding voltage level is applied across the motor phase winding as assigned below:

$$R1 \Rightarrow -(2/7)V_{dc};\ R2 \Rightarrow -(1/7)V_{dc};\ R3 \Rightarrow 0;\ R4 \Rightarrow (1/7)V_{dc};$$

$$R5 \Rightarrow (2/7)V_{dc};\ R6 \Rightarrow (3/7)V_{dc};\ R7 \Rightarrow (4/7)V_{dc};$$

$$R8 \Rightarrow (5/7)V_{dc}; \quad (16)$$

Three 120-degree phase shifted sinusoids with 20% third harmonics content are used as the reference waves for the proposed carrier based SPWM. The addition of third harmonic content increases the maximum fundamental voltage amplitude that can be generated using the SPWM scheme. These reference waves are continuously compared with the carrier set to determine the region (R1, R2…R8) in which the instantaneous value of the reference wave exists. This comparison is performed simultaneously for all the three phases.

Control signals for the two inverters then can be generated such that the appropriate devices are switched to realize the particular level in a particular phase depending upon the region. It may be noted that the proposed inverter can realize the even numbered levels also, and can start with the 2-level operation and progressively move to the 3-level, 4-level, 5-level, 6-level, 7-level and to the 8-level

operation as the modulation index increases. For low modulation index such that $V_m^* \leq V_C/2$ where Vm^* is the peak value of the modulating signal. The modulating signal at different instants could be in one of the eight regions R1, R2, R3, R4, R5, R6, R7 or R8. To realize the eight levels associated with these regions (equation 16), both inverters 'inverter-A' and 'inverter-B' would be switching (Table-II). If the reference wave is placed at the middle of the lowest carrier C1 as Fig.4(b), the modulating signal exists only in two regions R1 or R2 and it will result in only two levels L1 (-2/7 V_{dc}) and L2 (-1/7 V_{dc}). In this case the switching losses are only due to 'inverter-B'.

When the modulating index increases such that $V_C/2 \leq V_m^* \leq V_C$, an additional DC bias of $V_C/2$ is given to the reference wave such that it is at the middle of the two lower carriers C1 and C2 and results in 3-level operation (Fig.4(c)). A similar progressive DC shift in steps $V_C/2$ of is gives such that the inverter progressively moves through the 3-level, 4-level, 5-level, 6-level, 7-level and to 8-level operation. Fig.4(d) shows the reference wave corresponding to the maximum modulating signal. When the V/f control is used, these seven ranges of voltage amplitudes correspond to 7 ranges in frequency. Therefore the range (denoted by n = 1, 2, 3…7) in which the frequency command falls can be used to determine the DC shift to be given to the reference waves and the reference waveforms can be represented by,

$$V_a^* = V_m \sin wt + 0.2\, V_m \sin 3wt + n\, V_c/2, \quad (17)$$

$$V_b^* = V_m \sin(wt - 2\pi/3) + 0.2\, V_m \sin 3wt + n\, V_c/2, \quad (18)$$

$$V_c^* = V_m \sin(wt - 4\pi/3) + 0.2\, V_m \sin 3wt + n\, V_c/2. \quad (19)$$

When this SPWM scheme is employed, 'inverter-A' is clamped to zero level and 'inverter-B' is switched in three level mode to create the first three levels (L1, L2, L3), then 'inverter-A' is clamped to second level (2/7)V_{dc}, and 'inverter-B' is switched in 2-level mode to create the next two levels (L4, L5) and finally 'inverter-A' is clamped to its third level (5/7)V_{dc}, and 'inverter-B' is switched in 3-level mode to create the last three levels (L6, L7, L8). This results in the inverters, which has the higher DC bus voltage switching less frequently compared to the inverters having lower DC bus voltage.

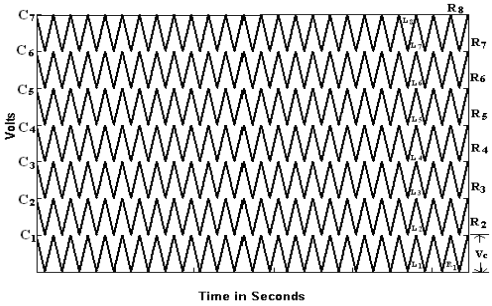

Fig.4(a). The carrier and the different regions in the multi carrier PWM

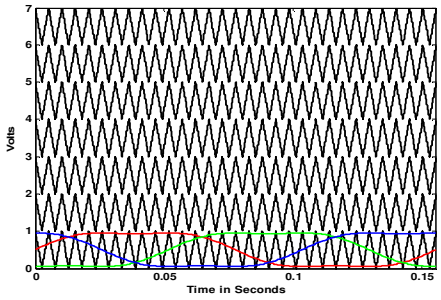

Fig.4(b). The reference wave set for 2-level operation in the proposed SPWM

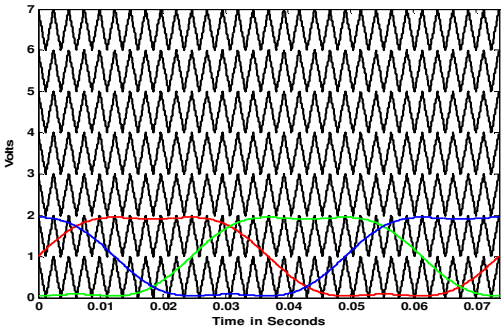

Fig.4 (c). The reference wave set for 3-level operation in the proposed SPWM

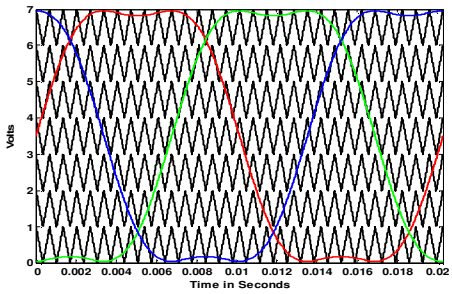

Fig.4 (d). The reference wave set for 8-level operation in the proposed SPWM

V. SIMULATION RESULTS AND DISCUSSION

The proposed scheme is simulated in open loop V/f control with multilevel carrier based SPWM using SIMULINK software in MATLAB environment. The respective DC-bus voltages are $(3/7)V_{dc}$, $(2/7)V_{dc}$, $(1/7)V_{dc}$ and $(1/7)V_{dc}$ for inverter-1, inverter-2, inverter-3 and inverter-4. This means that the DC-bus voltage of an equivalent conventional 2-level inverter drive is V_{dc}. The speed reference is translated to the frequency and voltage commands maintaining V/f. depending upon the range in which the frequency command falls the reference waves are generated according to Eqn. (17), (18) and (19). The three reference waves are simultaneously compared with the carrier set and the level at which the instantaneous value of the reference wave exists is determined.

A DC-bus voltage (V_{dc}) of 700 volts is assumed for simulation studies. A load torque of 10 N-M ia applied at 0.3sec. Fig.5 shows the motor phase voltage during 2-level operation. It may be noted that the inverter is operating in the 2-level mode. In this case 'inverter-B' is switched in the 2-level mode between $(2/7)V_{dc}$ and $(1/7)V_{dc}$ and 'inverter-A' is clamped to zero. Fig.6 shows the motor phase voltage during 3-level operation. The motor phase voltageV_{A2A4}, in the next speed range i.e. in 3-level operation with 'inverter-B' switching in the 3-level mode between $(2/7)V_{dc}$, $(1/7)$ V_{dc} and zero and 'inverter-A' is still clamped to zero. Fig.7 shows the motor voltage waveform in the next speed range in the 4-level operation, with 'inverter-A' switching in the 2-level mode between zero and $(2/7)V_{dc}$ and 'inverter-B' switched in the 3-level mode. Fig.8 shows the motor voltage waveform for the 5-level operation, where the 'inverter-A' switched in the 2-level mode between zero and $(2/7)V_{dc}$ and the 'inverter-B' is switched in the 3-level mode. Fig.9shows the motor voltage waveform in the 6-level operation in which the 'inverter-A' enters 3-level operation between $(5/7)V_{dc}$, $(2/7)V_{dc}$ and zero, and the 'inverter-B' switched in the 3-level mode between $(2/7)V_{dc}$, $(1/7)V_{dc}$ and zero. Fig.10 shows the motor voltage waveform in the 7-level operation. Fig.11 shows the motor voltage waveform in the 8-level operation.

It can be seen that the motor phase voltage during 8-level operation is very smooth and close to the sinusoid with lower THD. Fig.12a to Fig.12e show the phase voltage, transient phase current, steady state phase current, torque and speed of the motor during eight-level operation. Fig.13 shows the normalized harmonic spectrum of the motor phase voltage during 8-level operation. Fig.14 shows the decrease of total harmonic distortion (%THD) in the motor phase voltage as the number of levels increased.

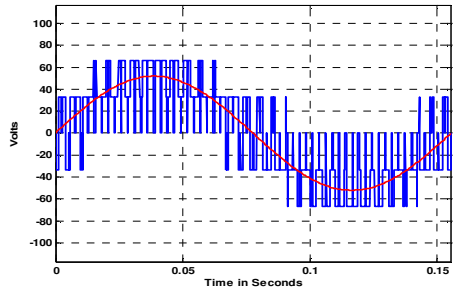

Fig.5.Motor phase voltage waveform during 2-level operation

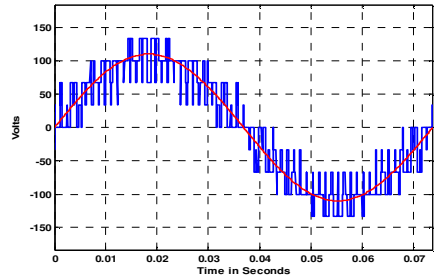

Fig.6. Motor phase voltage waveform during 3-level operation

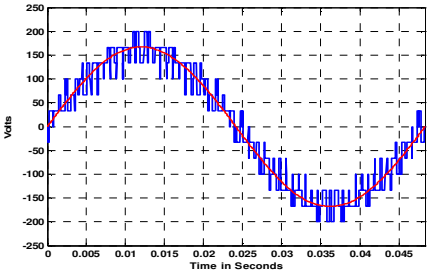

Fig.7. Motor phase voltage waveform during 4-level operation

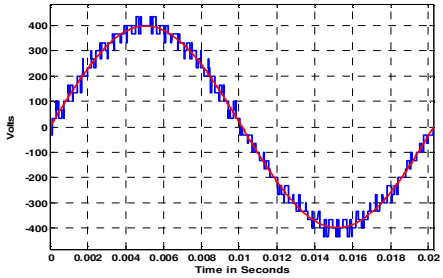

Fig.11. Motor phase voltage waveform during 8-level operation

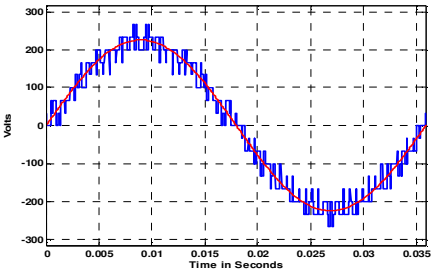

Fig.8. Motor phase voltage waveform during 5-level operation

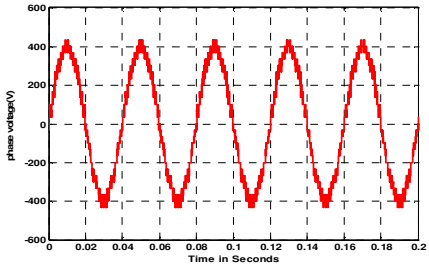

Fig.12a. Motor phase voltage during 8-level operation (with more number of cycles)

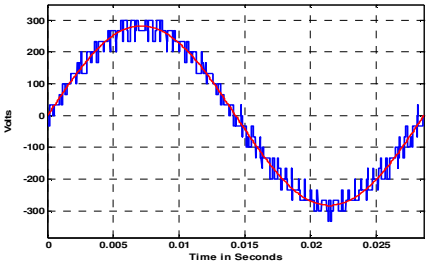

Fig.9.Motor phase voltage waveform during 6-level operation

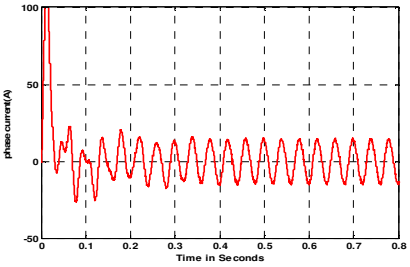

Fig.12b. Transient motor phase current during 8-level operation

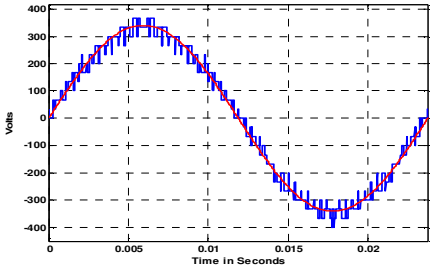

Fig.10. Motor phase voltage waveform during 7-level operation

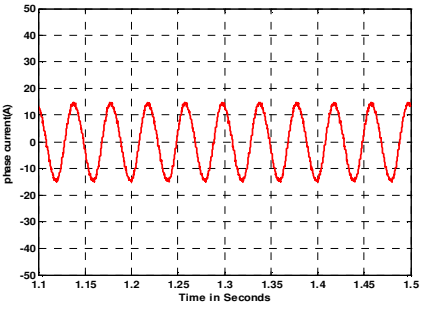

Fig.12c. Steady state Motor phase current during 8-level operation

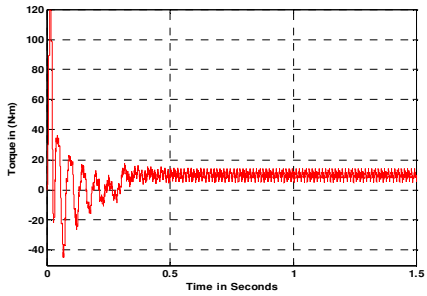

Fig.12d. Motor torque during 8-level operation

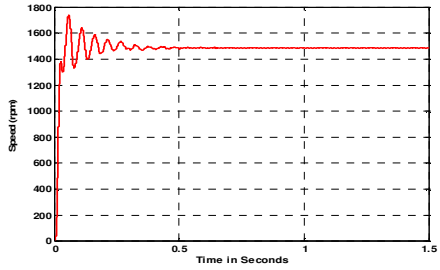

Fig.12e. Motor speed during 8-level operation

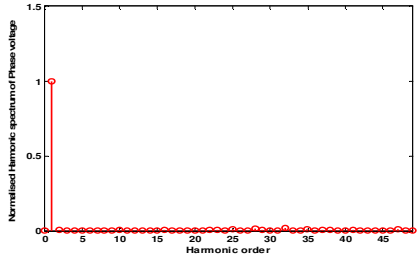

Fig.13. Normalized harmonic spectrum for the motor phase voltage during 8-level operation

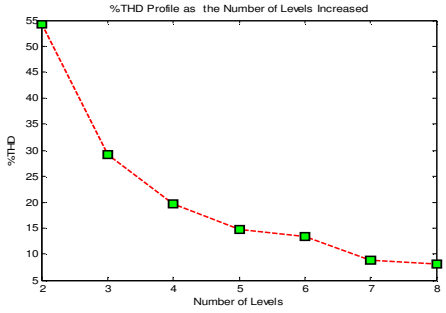

Fig.14. Total harmonic distortion (%THD) of the motor phase voltage as the number of levels increased

VI. CONCLUSION

Open-end winding induction motor fed by two 3-level inverters from both ends, results in voltage space phasor locations identical to a conventional 8-level inverter. The 3-level inverters used are realized by cascading two 2-level inverters. Comparing to the cascaded H-Bridge topology the present scheme employs a lower number of power supplies and switching devices. The proposed inverter does not experience neutral-point fluctuations and the DC-link capacitors carry only the ripple current as isolated DC supplies are used for all the DC links. The salient features of this scheme are:

- A multilevel carrier based PWM is only implemented for the drive topology for 8-level inverter, because of redundancy in switching states, the space vector modulation PWM is complex in identifying the appropriate switching state to minimize the harmonic content in the motor phase voltage waveform.
- This multilevel carrier based PWM eliminates the use of look up table approach to switch the appropriate space vector combination.
- The 8-level inverter offers improved motor phase voltage and phase current waveforms with low harmonic distortions than 5-level and 6-level inverter topologies.

The phase current is also near to sinusoidal and contains low THD. The motor torque reached steady state and responded for a change of load at 0.3 sec. The corresponding speed response is also presented and the speed reached the steady state. The motor exhibits good dynamic response. The phase voltage of eight-level operation contains lowest harmonics when compared to that of 2-level to 7-level operation. As the number of levels increased the %THD in the motor phase voltage decreased.

REFERENCES

[1] J-S. Lai; F. Z. Peng, "Multilevel converters-a new breed of power converters", *IEEE Transactions on Industry Applications,* Volume:32, Issue:3, May-June 1996, pp.509- 517.

[2] B. S. Suh, G. Sinha, M. D. Manjrekar, and T. A. Lipo, " Multilevel power conversion- An overview of topologies and modulation strategies," *OPTIM'98conference proceedings*, Brasov, Romania, September 1998, pp. AD11-AD24.

[3] F. Z. Peng, "A generalized multilevel Inverter topology with self voltage balancing," *IEEE Transactions on Industry Applications*, Vol 37, No.2, Mar/Apr. 2001, pp.611 - 616.

[4] P. M. Bhagawat and V. R. Stefanovic, "Generalised Structure of a Multi-level PWM inverter," *IEEE Transactions on Industry Applications*, Vol.1A-19, No.6, Nov/Dec 1983, pp.1057-1069.

[5] H. Stemmler, P. Guggenbach, "Configurations of high power voltage source inverter drives", *PE.Conference-1993*, Brighton, U.K., pp.7-12.

[6] E. G. Shivakumar, K. Gopakumar, S. K. Sinha, Andre Pittet, V. T. Ranganathan", Space vector PWM control of dual inverter fed open-end winding induction motor drive", *EPE Journal*, Vol. 12, no. 1, February 2002, pp.9 – 18.

[7] M. R. Baiju, K. K. Mohapatra, V. T. Somasekhar, K. Gopakumar and L. Umanand, "A five-level inverter voltage space phasor generation for an open-end winding induction motor drive", *IEE Proceedings on Electrical Power Applications*, Vol.150, No. 5,Sept 2003, pp: 531-538.

[8] V. T. Somasekhar, K. Gopakumar, "Three-level inverter configuration cascading two 2-level inverters", *IEE Proceedings –Electrical Power Applications*, Vol. 150, No. 3, May 2003, pp. 245-254.

[9] Y. Kawabata, M. Nasu, T. Nomoto, E. C. Ejiogu, T. Kawabata, "High-efficiency and low acoustic noise drive system using open-winding AC motor and two space-vector-modulated inverters", *IEEE Transactions on Industrial Electronics*,Volume:49, Issue: 4,Aug.2002,pp. 783 – 789.

[10] A. Rufer, M. Veenstra and K. Gopakumar, "Asymmetrical Multilevel converters for high resolution voltage phasor generation", *Conf. Proc. EPE'99*, pp.1-10.

[11] V. T. Somasekhar, K. K. Mohapatra, K. Gopakumar and L. Umanand and S. K. Sinha, **"**A multi level space phasor based PWM strategy for an open-end winding induction motor drive using two inverters with different DC link voltages", *Proceedings of 4th IEEE International Conference on Power Electronics and Drive Systems, 2001*, Vol. 1, 22-25 Oct.2001 pp. 169 – 175.

[12] M. R. Baiju, K. Gopakumar, K. K. Mohapatra, V. T. Somasekhar and L. Umanand, "A high resolution multilevel voltage space phasor generation for an open-end winding induction motor drive", *EPE Journal*, Vol. 13, No. 4, Nov. 2003, pp. 29-37.

[13] M. D. Manjrekar and T. A. Lipo, "A hybrid multilevel inverter topology for drive applications", *Conference proceedings of IEEE APEC 98*, pp.523-529.

[14] R. Lund, M. D. Manjrekar P. Steimer and T. A. Lipo, "Control strategies for hybrid seven level inverter", *in Proc. European Power Electronics Conf. (EPE'99),* Lausanne, Switzerland, 1999, CD-ROM.

[15] K.Chandra sekhar, G.Tulasi Ram Das, "An Eight-level Inverter System for an Induction Motor with Open-end Windings", in *Proceedings of the 2005 IEEE –PEDS Conference*, pp.219-223.

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