Current Reference Pierce Oscillator Circuit Topology for Low Phase Noise MEMS SAW Oscillator

Fazli Lut, Norlizawati Kamarudin and Jamilah Karim

***Abstract*— This paper presents the design and simulation of a current reference Pierce oscillator circuit topology for microelectromechanical systems (MEMS) based oscillator. The designed amplifier achieves a gain of 33 dB at VDD of 1.2V. The amplifier core was tested with surface-acoustic-wave (SAW) resonators range from 800MHz to 2.4 GHz to form an oscillator and it shows a phase noise level range of -146 dBc/Hz to -151 dBc/Hz at 100 kHz offset frequency. This satisfies the maximum requirements phase noise of local oscillator (LO) of ultra-high frequency (UHF) for Bluetooth technology and Global System for Mobile Communications (GSM). The device produced a better figure-of-merit (FoM) when compared with other oscillators that were based on CMOS on-chip inductor and capacitor (CMOS LC), film bulk acoustic resonator (FBAR) and lateral-field-excited (LFE) Aluminium Nitride (AIN) contour mode resonators technologies. The oscillator circuit has been simulated using a 0.13µm CL130G CMOS technology process from Silterra (Malaysia) with the oscillator core consuming only 1.07mW DC power.**

***Index Terms*— CMOS MEMS oscillator; Pierce oscillator; MEMS SAW resonator.**

I. INTRODUCTION

OSCILLATOR based on microelectromechanical systems (MEMS) are mostly used to generate the reference frequency and timing in electronic systems due to their small sizes and the potential to undergo fabrication with standard CMOS process, enabling novel single chip systems [1]–[3] with higher frequency suitable for wireless communications. High capacitive behavior of the resonator's source and load impedances in Pierce oscillator circuit allowed this topology to produce very good short-term stability as well as providing a large output signal and drives the resonator at low power levels. The oscillation frequency was relatively insensitive to small changes in the series resistance or shunt capacitances because of the large phase shift in *RC* networks and large shunt capacitances. The *RC* network and shunt capacitances to ground allowed Pierce oscillator circuit to have high immunity to noise [4].

In our previous work, we presented the first Pierce oscillator circuit topology for MEMS SAW resonators, employing MIMOS 0.35um CMOS process [5]. The design yields an 18 dB gain and consumes 3.18 mW power with 3V supply.

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This paper presents the design and simulation of CMOS MEMS oscillator with current reference base oscillator circuit for MEMS SAW resonator. Three resonators with different resonant frequencies ranging from 800 MHz to 2.4 GHz were used to test the oscillator. Section II presents the general discussion on the oscillator system. Section III explains the implementation of MEMS oscillator and the discussion of the output from the simulation process with Section IV concluding the paper.

II. ELECTRICAL MODEL OF SAW RESONATOR

Fig. 1 shows the equivalent circuit model for SAW resonator [6]. The fundamental parameter such as R_x, C_x, L_x and C_f defines the acoustic components while C_1 and C_2 are the parasitic components. In addition to that, R_x which is known as "motional resistance" will generally determine the quality factor and insertion loss of the resonator. In terms of the piezoelectric vibrator, at a given frequency as the amplitude of vibration is approaching zero, the parameters of the equivalent will generally approach constant values [6]. Meanwhile, parasitic components exists due to the structure of transducer of the resonator formed using the composite of Aluminium (Al) and Silicon dioxide (SiO_2) layers [7].

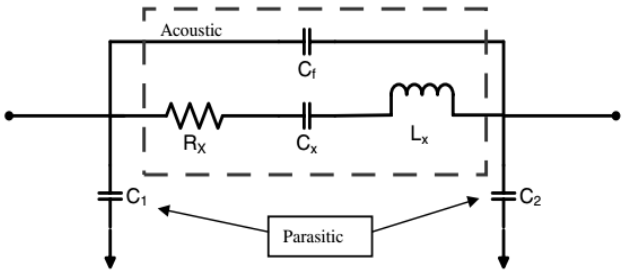


Fig.1 Equivalent circuit model for SAW resonator [5]

Table I shows the parameters specification for three different SAW resonators with different resonant frequency used to test the Pierce oscillator circuit topology.

TABLE I. RESONATOR SPECIFICATION

Elements	Resonator		
	869 MHz	916 MHz	2.44 GHz
R_X	12.7	16	15.5
L_X (µH)	19.757	19.99	2.80
C_X (fF)	1.7	1.513	1.52

Elements	Resonator		
	869 MHz	916 MHz	2.44 GHz
C_f (pH)	2.70	1.50	0.67
f_S (GHz)	0.87	0.91	2.40
Q(typical)	8500	8000	2800
IL (dB)	1.7	1.7	2.2

R_x = motional resistance; L_x = motional inductance; C_x = motional capacitance; *C_f = parallel capacitance; f_s = resonant frequency; Q = unloaded quality factor;* IL = *insertion loss*

III. Pierce Oscillator Circuit Design

Fig. 2 shows the current reference Pierce oscillator circuit topology designed. In order to provide the startup and stable oscillation, the circuit topology chosen must have a gain greater or equal than 1 and 0º or 360º phase shift to satisfy Barkhausen criteria for the oscillation [8]. The oscillator design in this work was implemented using the 0.13µm CL130G CMOS technology from Silterra. This Pierce oscillator was chosen because the topology is simple and provides a straightforward biasing. Besides that, it has superior performance in terms of low power consumption and phase noise characteristics.

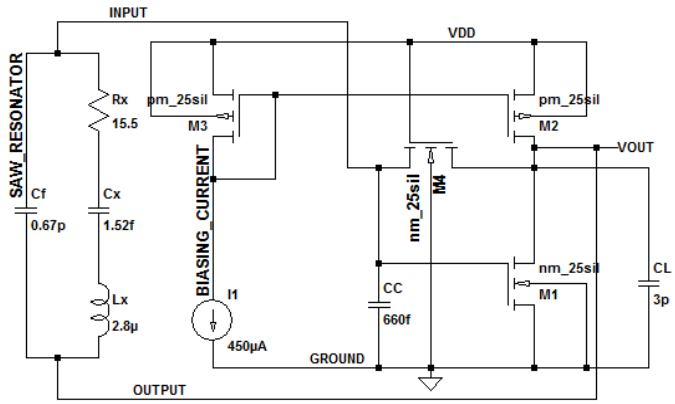


Fig. 2 Transistor-level circuit schematics of pierce oscillator circuit topology

Based on Fig. 2, the Pierce oscillator core shown is basically a CMOS-inverting amplifier consisting of transistors M1 and M2. Transistor M4 is biased at the triode region to make it behaves like a large resistor. The purpose of this ohmic transistor of M4 is to bias and manipulate the gate and drain voltages of transistors of M1 and M2 at 0.5% of VDD and minimize the resistive loading on the resonator. This implementation will also help to improve and maximize the allowable oscillating voltage swing of the circuit. From Fig. 2, the bias current for the transistors in the inverting amplifier can be controlled from the outside and thus allow this circuit to be suitable for having multi-frequency resonators driven by the same oscillator core. The goal of having this multi-frequency is also supported by the tunable supply voltage V_{DD}. The DC bias current of M1 was reused in M2 and this summed up the AC gain of the transistors. The total transconductance (g_m) of transistors in circuit shown in Fig. 2 can then be expressed as:

$$g_m = g_{m1} + g_{m2} + g_{m3}$$

$$= |\mu_n| Cox \left(\frac{W}{L}\right).\left(\frac{Vdd}{2} - |V_{TN}|\right) + |\mu_n| Cox \left(\frac{W}{L}\right).\left(\frac{Vdd}{2} - |V_{TP}|\right) + |\mu_p| Cox \left(\frac{W}{L}\right).\left(\frac{Vdd}{2} - |V_{TP}|\right) \quad (1)$$

where μ_n and μ_p is the electron mobility and hole mobility respectively; *Cox* is the capacitance per unit area of the gate oxide; V_{TN} and V_{TP} is the threshold voltage of N-type metal-oxide-semiconductor (NMOS) and P-type metal-oxide-semiconductor (PMOS) transistors respectively while *W/L* are the width-to-length ratios for transistors M1, M2 and M3. Table II shows the parameters used to determine the transistor sizing for the circuit. The minimum value of length of the transistors used in this circuit was 0.32µm and satisfies the requirement of minimum length for 0.13µm CL130G Silterra technology process which was 0.28µm. This is important to ensure that there will be no error during the layout process.

TABLE II. CMOS DESIGN PARAMETERS

Parameters	0.13µm CL130G Silterra	
	Value	*Unit*
$\mu_n C_{ox}$	344.4	µA/V
$\mu_p C_{ox}$	121.3	µA/V
V_{DD}	1.2	V
W_1/L_1	29.4/0.32	µm/µm
W_2/L_2	12/0.32	µm/µm
W_3/L_3	12/0.32	µm/µm
W_4/L_4	50/100	µm/µm
C_c	660	fF
C_L	3	pF

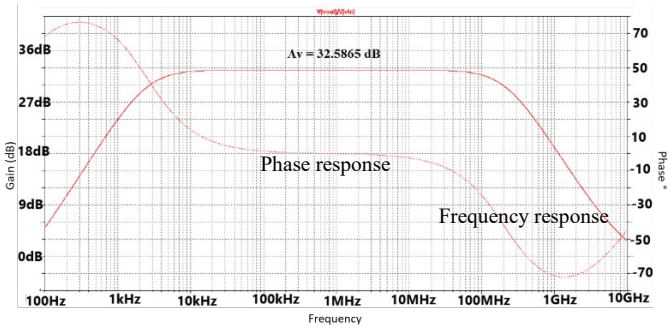
Transistor M1 was designed from the factor of gain-bandwidth (GBW) needed for the circuit and the small signal transconductance g_{m1} from gate to channel. In order to ensure that the circuit was able to operate at high gigahertz frequency range, 3 GHz was chosen as the value of GBW as the highest resonance frequency desired for the circuit is 2.4 GHz. The transistor's width of M2 and M3 were optimized from 5.5µm to 12µm in order to increase the size of bandwidth of the circuit. Clearly, the width and length of M_4 is optimized from 4µm to 50µm and 10µm to 100µm respectively so that the transistor behaved as a large resistor in the oscillator circuit. Meanwhile, the biasing current used in the oscillator circuit is 450µA to ensure the transconductance, g_m yield from the pierce oscillator circuit will provide enough gain for the oscillation to sustain.

The two capacitances, CL and CC in the Pierce oscillator circuit can be utilized to compensate the parasitic in the circuit. In analog circuit design, the existence of parasitic capacitance will produce extra phase shift where this situation must be carefully observed into the design work to ensure that the designed oscillator works properly. In Fig. 2, the parasitic capacitance is usually located at the input and output of the resonator as shown. The existence of parasitic capacitance in the circuit may be due to the transistors in amplifier, bond-pads, bond-wires, parasitic in the resonator and the resonator's bias circuit. In order to avoid degrading of frequency stability and to

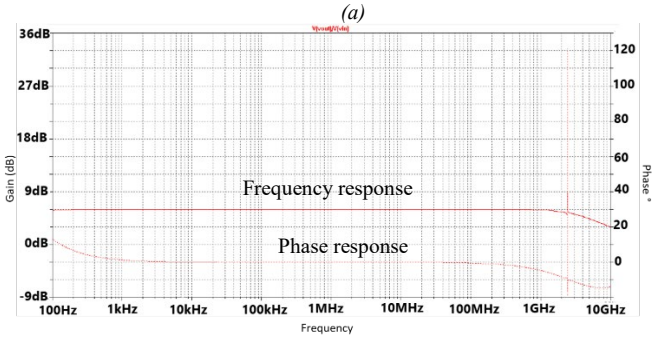
increase the current in the circuit, transistors M1 and M2 in the inverter amplifier needs to be biased with very high value of resistor [4]. This can be done by putting one of transistor that operates in the triode region connected to the gate and drain of the biasing transistors respectively. At this triode region, this transistor will behave like a resistor [9] in the oscillator circuit.

IV. SIMULATION RESULTS

Fig. 3 shows the simulation results of the frequency and phase response for the amplifier and also the results when the 2.4 GHz resonator was connected to the amplifier. The topology yields the open loop gain and phase, $A_v = 32.5865\ dB$ and $\angle A_v = \angle 70.42°$. The gain and phase obtained is enough to make the circuit oscillate at the resonance frequency since it has obeyed the Barkhausen criteria for oscillation. Since the insertion loss (IL) of the resonators as written in Table 1 are 1.7 and 2.1 only. Thus, the gain obtained from the designed circuit are able to overcome the IL of the resonator



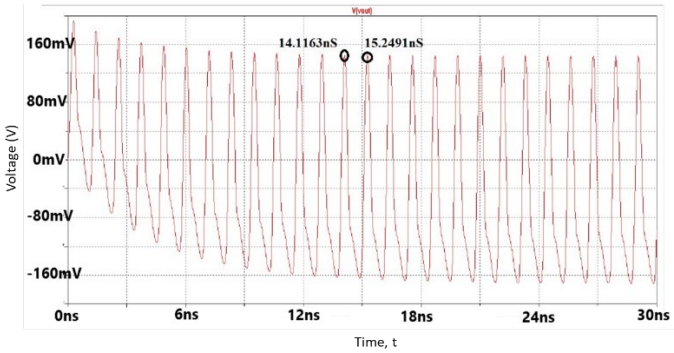
(a)



(b)

Fig. 3 Frequency and phase response (a) amplifier (b) amplifier tested with 2.4-GHz SAW resonator

Fig. 4 shows the transient response of the MEMS based oscillator with 869 MHz, 916 MHz and 2.4 GHz resonator. The period output signal of the simulation for 868 MHz, 914 MHz and 2.4 GHz is 30ns. Oscillators 868 MHz, 914 MHz and 2.4 GHz took 9ns to reach stable oscillation. Thus, the pierce oscillator circuit designed can sustain the oscillation from the 868 MHz, 916 MHz and 2.44 GHz resonators.



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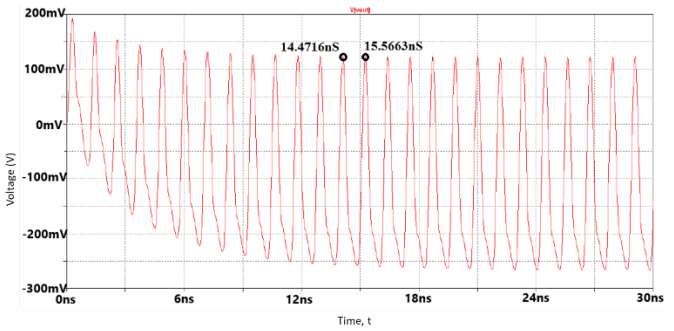

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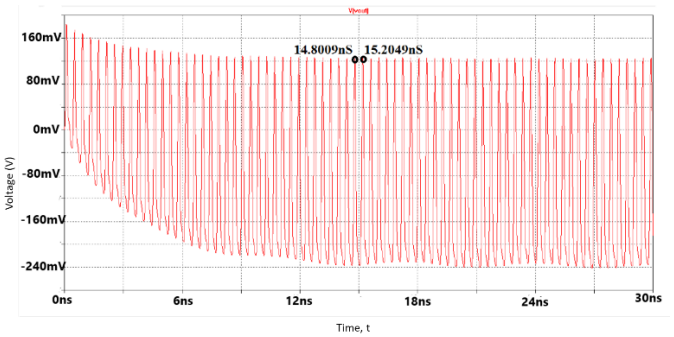


(c)

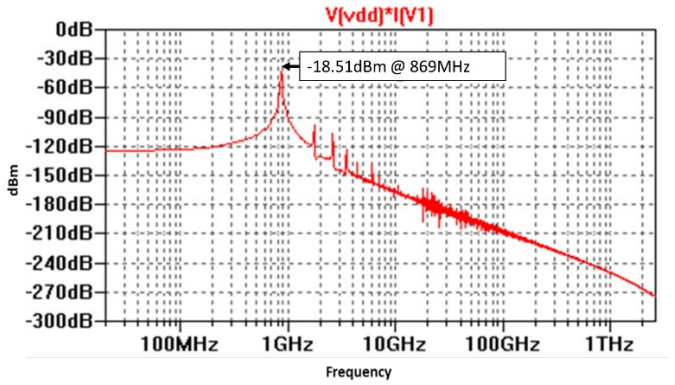
Fig. 4 Simulated frequency oscillation of CMOS MEMS SAW (a) 868 MHz (b) 914 MHz (c) 2.44 GHz

Fig. 5 shows the periodic steady state output for each of the MEMS based oscillator tested with different resonators and this was obtained using Fast Fourier Transform (FFT) spectrum analyzer simulation. The output power spectrum of the oscillation is calculated using equation (2):

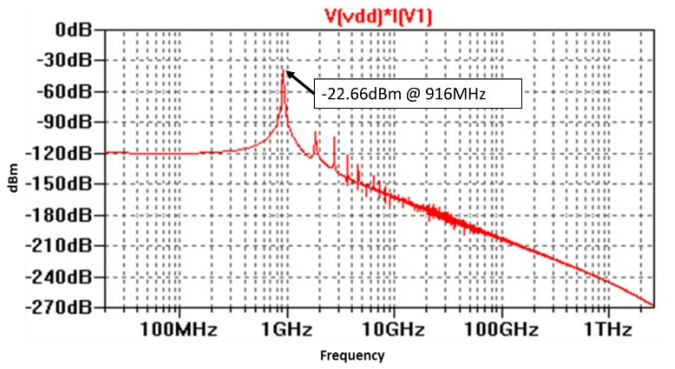
$$10log\frac{Pdiss}{1mW} = dBm \qquad (2)$$

where P_{diss} is the power dissipation at resonance frequency level. Thus, the phase noise output for all the three oscillators at 100 kHz cut off frequency is summarized in Table III. As observed in Table III, Pierce oscillator based on MEMS SAW resonators have demonstrated the phase noise values between -146 dBc/Hz to -151.6 dBc/Hz at 100 kHz offset frequency. Oscillator 869 MHz has lowest phase noise and oscillator 2.44 GHz. The 2.4 GHz oscillator has the highest phase noise value

since the quality factor of the 2.44 GHz is the lowest as reported in Table I.



(a)



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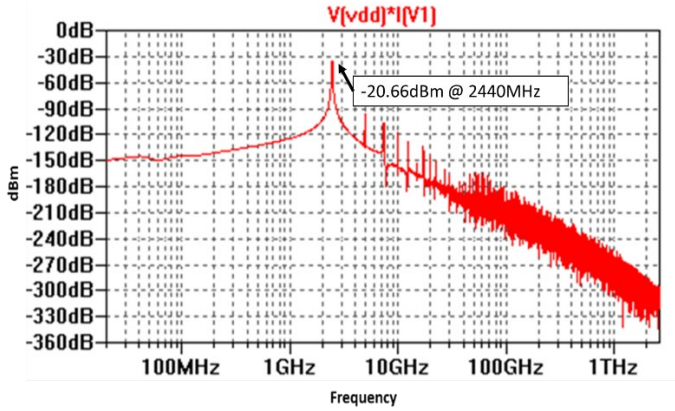

(c)

Fig. 5 Periodic steady state output (a) 868 MHz (b) 914 MHz (c) 2.44 GHz

TABLE III. PHASE NOISE OF OSCILLATOR BASED ON DIFFERENT RESONATOR

Elements	Resonator		
	868 MHz	**915 MHz**	**2.44 GHz**
Phase Noise (dBc/Hz)	-151.6 @ 100 kHz	-150.8 @ 100 kHz	-146 @ 100 kHz

From Table III, the 868 MHz MEMS based oscillator shows the best phase noise performance as compared with other oscillators with different resonator. The phase noise simulation was compared with the GSM and Bluetooth requirements of UHF LO [10]. Based on the results obtained, the phase noise performance of the designed oscillator already satisfies the requirement of Bluetooth technology, which is -110dBc/Hz at 500 kHz frequency offset, GSM850/900 requirements which is -138dBc/Hz at 600 kHz frequency offset and DCS1800/1900 requirements which is -135dBc/Hz at 3 MHz offset.

The overall performance of the designed oscillator was then compared with other gigahertz oscillators based on different technologies by using figure-of-merit (FoM) given by the following equation (3) [11]:

$$FoM = L(f_m) - 20\log(\frac{f_o}{f_m}) + 10\log(\frac{P_{diss}}{1mW}) \quad (3)$$

where L (f_m) is the oscillator phase noise at specific offset frequency; f_o is the carrier frequency; P_{diss} is the DC power consumption (in milliwatts) of the oscillator circuit. Table IV shows the calculated FoM values for gigahertz oscillator based on different technologies. As shown in Table IV, MEMS oscillator demonstrated in 0.13µm CL130G Silterra with 2.4 GHz SAW resonator has the best FoM when compared with other oscillator based on LFE and FBAR.

TABLE IV. FOM COMPARISON OF GHZ OSCILLATORS BASED ON DIFFERENT TECHNOLOGIES

References	Parameters			
	f_o **(GHz)**	***Phase Noise (dBc/Hz)***	P_{diss} **(mW)**	**FoM (dBc/Hz)**
[4]	2	-144 @ 1 MHz	0.6	-212
[12]	1	-140 @ 100 kHz	3.5	-215
[13]	1	-156 @ 600 kHz	9.4	-210
This work	2.4	-146 @ 100 kHz	1.07	-249

V. CONCLUSION

The Pierce oscillator circuit topology with current reference base has been chosen as a sustaining circuit for the oscillator based on MEMS SAW resonator. The circuit has been designed and simulated using 0.13µm CL130G Silterra CMOS technology process. The 2.4 GHz MEMS based oscillator shows the best phase noise performance among other oscillators with different resonator with a phase noise of -181 dBc/Hz at 1 MHz offset frequency and phase noise floor of -182 dBc/Hz, which it satisfies the Bluetooth and GSM requirements for UHF LO. In addition to that, the overall performance of 2.4 GHz oscillator has the best FoM when compared with other gigahertz oscillators that are based on FBAR, AIN-Contour Mode-

MEMS and CMOS LC technologies. In future studies, expanding this oscillator technology to microwave frequency would be desired.

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