Modeling of "Strain Technology" on 140nm CMOS Devices

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Abstract—**A 140nm Complementary Metal Oxide Semiconductor (CMOS) was designed and simulated to investigate stress effects on device performance. Stress can be divided into two categories which are compressive and tensile stress. Strain technology is capable to introduce stress to the CMOS devices. The strain technology can be developed by Silicon Nitride (Si_3N_4) capping layer, Silicide and Shallow Trench Isolation (STI). The paper discussed on the effect of strain technology on 140nm CMOS device performance focusing on threshold voltage and drain current parameters. ATHENA and ATLAS simulators were used to simulate the fabrication process and to characterize the electrical properties respectively. It can be concluded that STI is better compared to LOCOS for length gate below than 250nm devices. Compressive STI stress enhances by 13.8% PMOS performance while tensile Si_3N_4 capping layer improve by 1% NMOS performance. In addition CMOS with silicide module improve by 2.5% PMOS drain current.**

Index Terms— **Compressive stress, Tensile stress, Nitride (Si_3N_4) capping layer, Silicide, Shallow Trench Isolation (STI)**

I. Introduction

Stress will be developed between two films which have (or a film in substrate) different coefficients of thermal expansion are in contact of each other. Generally, heating or cooling one film will minimize or expand the film more than the other [1]. Stresses are divided into two types which are tensile stress and compressive stress.

Tensile stress is the stress in which the two sections of material on either side of a stress plane tend to pull apart or elongate. Compressive stress is the reverse of tensile stress which is adjacent parts of the material tends to press against each other [2].

Figure 1 illustrates tensile and compressive stress cross section on CMOS. Applied stress to the channel significantly improves CMOS device performance in terms of current and carrier mobility. The best method that can enhance the performance of CMOS devices is strain silicon technology [6]. In order to produce strain, several approaches have been used like Shallow Trench Isolation (STI), Silicidation process, Silicon Nitride (Si_3N_4) Capping Layer and SiGe (Silicon Germanium) in the source/drain regions. In this paper, several technology had been covered which are STI, Silicidation process and Si_3N_4 capping Layer

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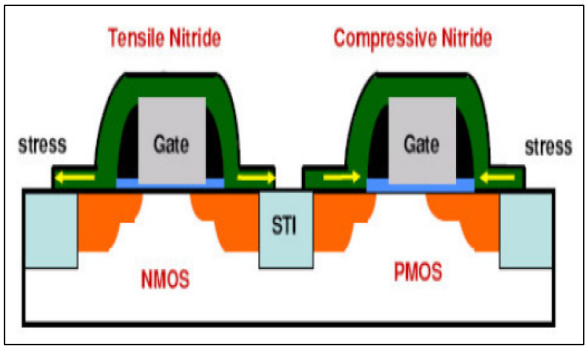


Fig. 1: Tensile and compressive stress. (Extracted from N. Mohta and S.E. Thompson, "Strained Si-The Next Vector to Extend Moore's Law").

A. *Shallow Trench Isolation (STI)*

Compressive strain is resulted by STI when ones increase the channel region and decrease the distance between STI edge and transistor. Figure 2 shows the resultance structure of compressive strain using STI. The compressive stress is induced when cooling down from high temperature at the trench fill. The different Coefficients of Thermal Expansion (CTE) between silicon substrate and STI oxide contributes a compressive lateral stress from oxide to silicon in the active area of the transistor. Compressive stress in Metal Oxide Semiconductor Field Effect Transistor (MOSFET) channel changes the device performance of each type of transistor [3]. STI compressive stress causes NMOS drain current (I_d) to degrade and PMOS I_d to increase. The STI stress has more significant effects on I_d mismatch of short channel transistor compare to the long channel transistors. This is because STI stress has higher effect on short channel compare to long channel I_d [4].

STI stress compresses the transistor channel in two directions. When the stress is in the direction of channel length, it is known as x-stress (tensile stress) which is good

for NMOS devices and when the stress in the direction of channel width it is known as y-stress (compressive stress) [5]. The y stress is good for PMOS devices.

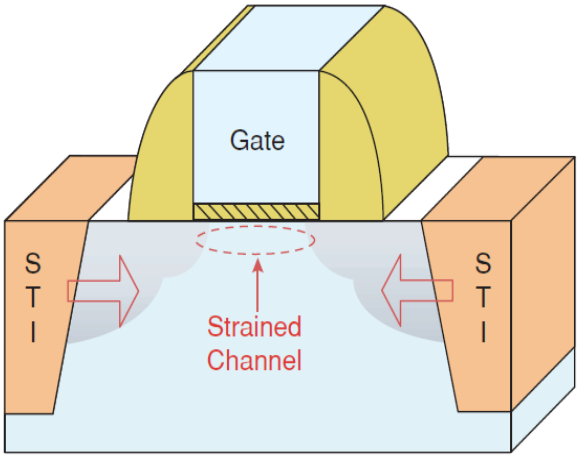


Fig.2: STI to create compressive strain in PMOS. (Extracted from Chee Wee Liu, S. Maikap and C.-Y. Yu "Mobility Enhancement Technologies").

B. *Silicon Nitride (Si_3N_4) Capping Layer*

Silicon nitride (Si_3N_4) capping layer produce a high level of stress. Si_3N_4 film can have either tensile or compressive strain depending on the deposition technique. Si_3N_4 drive currents for both n- and p-channel MOSFETs can be improved by controlling the stress of the Si_3N_4 layer selectively [6]. A tensile Si_3N_4 capping layer used to create a stretched NMOS channel as shown in Figure 3.

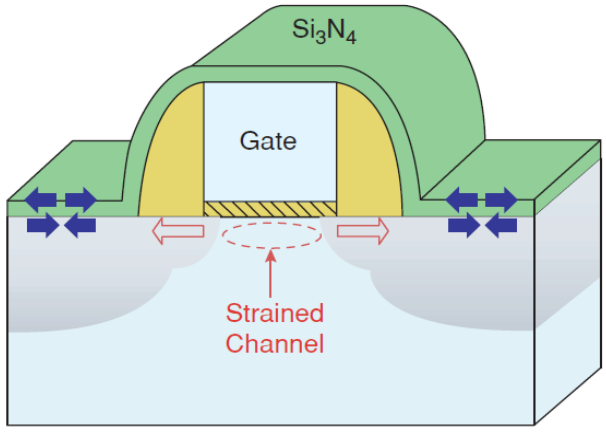


Fig.3: Si_3N_4 capping layer to create tensile strain in NMOS. (Extracted from Chee Wee Liu, S. Maikap and C.-Y. Yu "Mobility enhancement Technologies").

The tensile capping layer deposited by thermal chemical vapor deposition (CVD) can improve the performance of NMOS due to the induced tensile strain in the channel region while the compressive capping layer deposited by plasma enhanced CVD can improve the PMOS due to the induced compressive strain in the channel region. Si_3N_4 capping layer with high tensile strained can improve NMOS performance but degrade PMOS performance [7].

The device current will improve up to 25% by increasing the thickness of tensile Si_3N_4 layer. However, the thickness of Si_3N_4 becomes saturated at 100nm thick and I_{dsat} gain is also limited. Furthermore, thicker Si_3N_4 capping film causes wafer bending. This bending causes wafer crash in process instruments and disables the focus control for photo steppers. And it also degrades the PMOS drive current [8].

C. *Silicide*

Metal silicides such as nickel silicide ($NiSi_2$) and tungsten silicide (WSi_x) can be used to obtain compressive stress in the PMOS channel as a shown in Figure 4. The formation of metal silicides (such as WSi_2 and $TiSi_2$) in Very Large Scale Integrated (VLSI) circuits can generally be accomplished in four ways which are by deposition of the pure metal into an Si layer (which can be the single-crystal substrate or poly-crystalline Si), simultaneous evaporation of the silicon and the refractory metal from two sources, sputter deposition of the silicide either from a composite target or by co-sputtering and chemical vapor deposition (CVD). Silicides have a higher thermal coefficient of expansion than Si and patterning them on the top of the PMOS transistors structure squeezes the Si channel underneath leading to higher hole mobility [9].

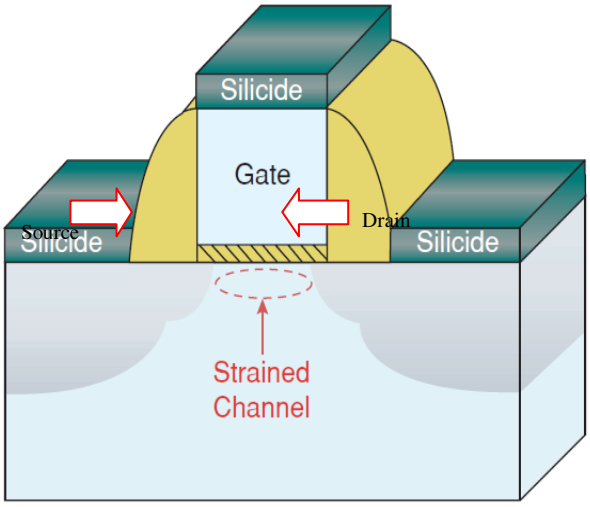


Fig. 4: Silicide for compressive strain in PMOS. (Extracted from Chee Wee Liu, S. Maikap and C.-Y. Yu "Mobility enhancement Technologies").

The advantages of using silicide are low temperature silicidation process, low silicon consumption, smaller mechanical stress, good contact to other material and little or no electromigration.

The common silicides ($TiSi_2$, WSi_2, $CoSi_2$, and NiSi) have larger thermal expansion coefficient than Si and yield

compressive Si underneath. However, when the stress exceeds the critical shear stress and hence the dislocations detrimental to the devices performance.

Silicide-induced tensile strain in the channel has enhanced both NMOS and PMOS transconductance as the source drain width scales [10].

II. METHODOLOGY

The design process and device modeling for this research was done by using TCAD SILVACO software. The structures of the simulation were simulated from ATHENA window, while the characteristic of the structures was simulated from ATLAS.

A. ATHENA And ATLAS Simulation

ATHENA is a process to develop and optimize semiconductor. ATHENA process simulators are used in creating CMOS device structure.

The recipe is simulated and the variable such as temperature, time and material are varied in order to get threshold voltage and other parameters in acceptable range and the structure of NMOS and PMOS. The device structure can be view using Tonyplot. The processes that involve in fabrication are layer deposition, lithography, etching, implantation, oxidation and diffusion.

ATLAS is a physical-based two dimensional device simulator. It predicts the electrical behavior of specified semiconductor structures, and provides insight into the internal physical mechanisms associated with device operation. ATLAS will simulate the electrical characteristics of the CMOS structure that was created by ATHENA. ATLAS generates I_d-V_d curve, I_d-V_g curve and hence producing threshold voltage (V_t) and drain current (I_d). Figure 5 show the flow of the simulation.

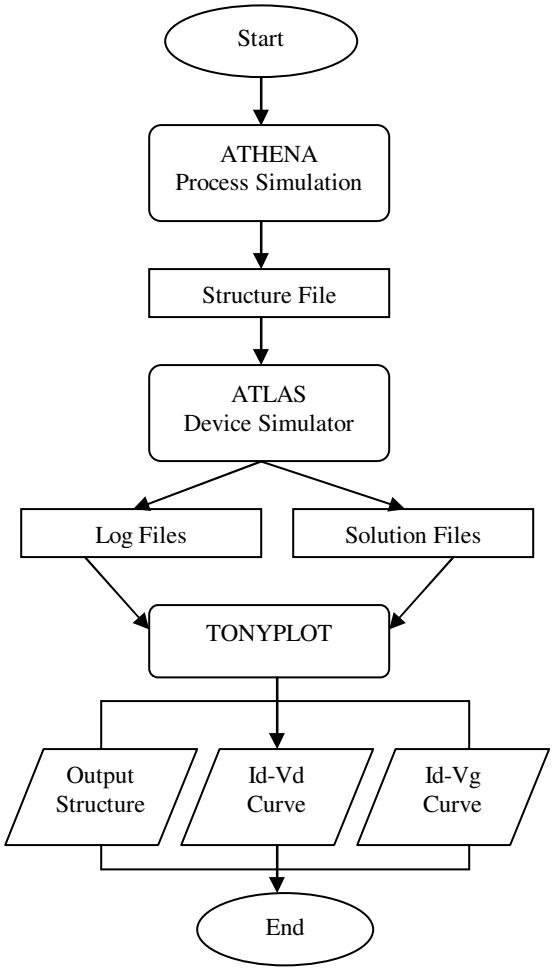


Fig.5: Modeling flow chart

III. RESULTS AND DISCUSSION

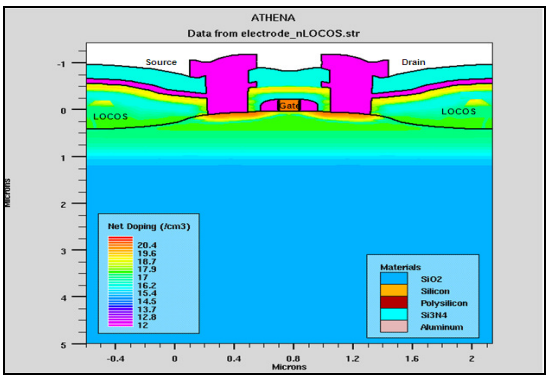
Figure 6 (a) and (b) shows the cross section of 140nm NMOS with different method isolation. Figure 7 shows the electrical characteristic curve for NMOS. Figure 7(a) is I_d-V_d curve where the voltage gate is set to 1V, 2V and 3V. The drain current at gate voltage 3V is 1.46mA. Figure 7(b) is shows the I_d-V_g curve where the drain voltage is set to 0.1V. From the figure 7(b), ones can determine the threshold voltage values. The drain current and the threshold voltage values can be calculated using equation 1 and 2 respectively.

$$I_{Dsat}=\frac{WC_{OX}\mu}{L}\left[\left(V_{GS}-V_T-\frac{V_{DSAT}}{2}\right)V_{DSAT}\right] \quad (1)$$

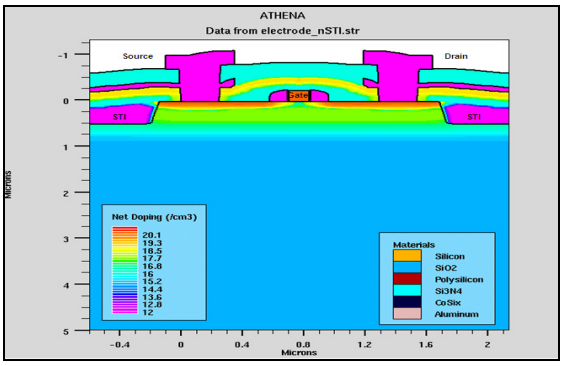
$$V_T = V_{GS(0)}-\frac{V_{DS}}{2} \quad (2)$$

A. Electrcal Characteristic of 140nm CMOS

Table 1 shows the electrical characteristic of CMOS between different isolation techniques. Both conventional LOCOS and STI were compared. Result showed that STI is better compared to the LOCOS. These verify that STI technology is suitable for gate length of 140nm. In addition the process of STI technology is more simple and low cost.

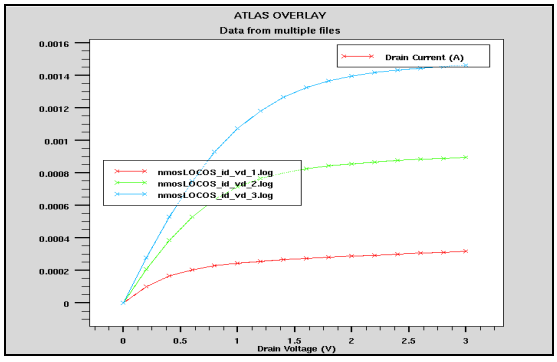


(a)

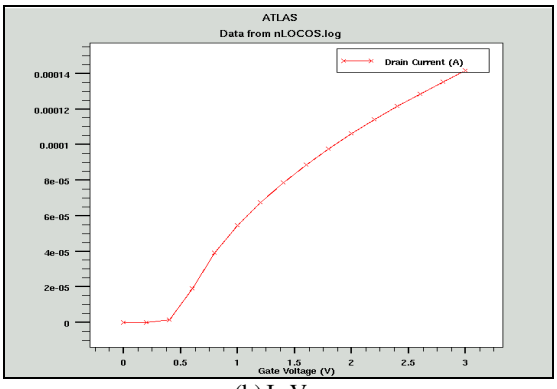


(b)

Fig. 6: Cross section of 140nm NMOS with different isolation: (a) LOCOS (b) STI



(a) I_d-V_d curve



(b) I_d-V_g curve

Fig.7: Electrical characteristic curves fpr NMOS in (a) and (b).

TABLE I
ELECTRICAL CHARACTERISTIC OF CMOS WITH DIFFERENT ISOLATION TECHNIQUES.

	Vt (V)		*I_d (mA)*	
	NMOS	PMOS	NMOS	PMOS
LOCOS	0.372	-0.133	1.46	-0.738
STI	0.240	-0.234	1.47	-0.840

Equation 3 shows the comparison percentage between LOCOS and STI focusing on drain current characteristic. It is observed that PMOS is having better performance compared to NMOS since the PMOS drain current is increasing by 13.8% with an introduction of STI. STI is generating compressive stress to the device and therefore increases the drain current of PMOS and degrades the NMOS drain current performance. In summary, compressive STI stress favors to PMOS mobility but not to NMOS. Thus, a selective modification of STI stress effect is important for advanced NMOS.

$$Variation\ of\ Drain\ Current = \frac{I_{d\,STI} - I_{d\,LOCOS}}{I_{d\,LOCOS}} \times 100\% \quad (3)$$

A. *Silicon Nitride (Si_3N_4) Capping Layer*

Table 2 shows the electrical characteristic of CMOS with different thickness of Si_3N_4 capping layer for both STI and LOCOS technology. For this research, 20nm and 80nm thick of Si_3N_4 capping layer were used to compare the electrical characteristic performance.

TABLE 2
ELECTICAL CHARACTERISTIC WITH Si_3N_4 CAPPING LAYER

	Si_3N_4 thickness	*Vt (V)*		*I_d (mA)*	
		NMOS	PMOS	NMOS	PMOS
LOCOS	20nm	0.373	-0.133	1.470	-0.780
	80nm	0.372	-0.133	1.460	-0.779
STI	20nm	0.241	-0.232	1.460	-0.840
	80nm	0.240	-0.231	1.460	-0.830

From the table, it shown that Si_3N_4 capping layer has no significant effect on electrical characteristic with the changes of the thickness of Si_3N_4. For NMOS with LOCOS technology for 20nm Si_3N_4 capping layer thick the I_d is 1.47mA while for 80nm Si_3N_4 capping layer the current is only 1.46mA. In addition, for NMOS with STI technology there is no changes of current reported. I_d for NMOS LOCOS technology degrades about 1% but this is not significant. Si_3N_4 capping layer cannot be too thick because it can cause wafer bending and thus will cause wafer broken.

The electrical characteristics of CMOS with Si_3N_4 capping layer were compared to the electrical characteristic without Si_3N_4 capping layer. Figure 8 and 9 shows the comparison of NMOS and PMOS with and without Si_3N_4 capping layer.

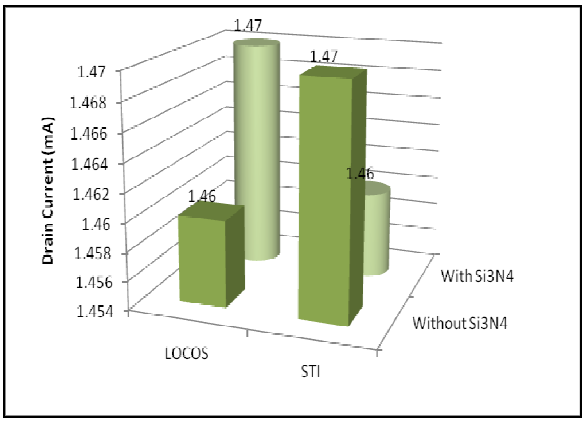


Fig. 8: Drain current comparison of NMOS between with and without Si_3N_4 capping layer.

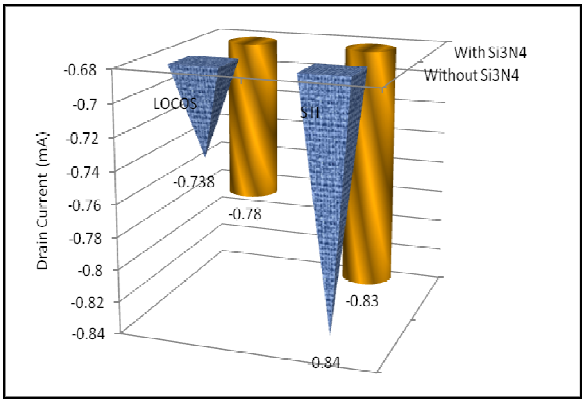


Fig. 9: Drain current comparison of PMOS between with and without Si_3N_4 capping layer.

NMOS has not shows significant changes but PMOS obviously shows changes. NMOS for LOCOS technology shows enhance performance but for STI technology shows degrade performance. For PMOS LOCOS technology shows 5.7% improvement but STI technology shows 1% decreases. For LOCOS technology, it is shows that Si_3N_4 capping layer improve NMOS performance but degrade PMOS performance while STI technology improve PMOS performance but degrade NMOS performance. It can be concluded that LOCOS technology having high tensile stress and STI technology having high compressive stress.

B. Silicide

Table 3 shows the electrical characteristic of CMOS with silicide. From the table it shows that CMOS with STI technology having a higher I_d. Drain current for both NMOS and PMOS were improve. NMOS increase 1.4% while PMOS improve 16.5%.

TABLE 3
ELECTRICAL CHARACTERISTIC WITH SILICIDE

	Vt (V)		*I_d (mA)*	
	NMOS	PMOS	NMOS	PMOS
LOCOS	0.372	-0.133	1.44	-0.738
STI	0.240	-0.255	1.46	-0.860

Both NMOS and PMOS with silicide and without silicide electrical characteristic were compared. Figure 10 shows the comparison of NMOS with silicide and without silicide while figure 11 shows the comparison of PMOS with and without silicide.

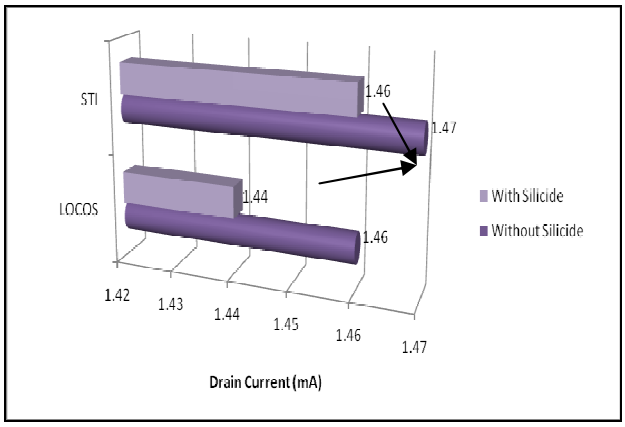


Fig.10: Comparison of NMOS between with and without Silicide.

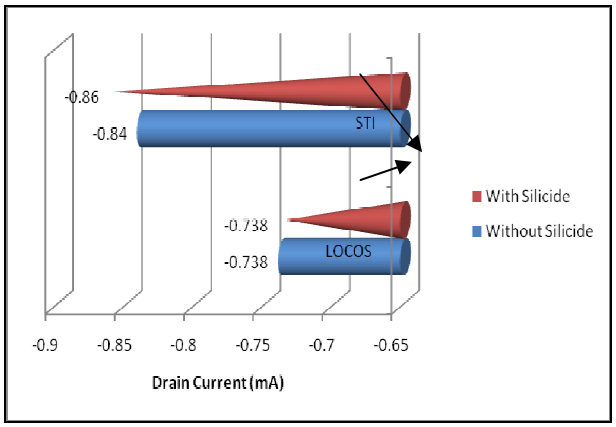


Fig. 11: Comparison of PMOS between with and without Silicide.

For NMOS both LOCOS and STI technology shows decrease performance. Both technology decrease about 1%. However, PMOS was shows the improvement. PMOS with LOCOS technology shows not significant changes but PMOS with STI technology improve about 2.5% performance. PMOS induced compressive stress therefore it shows increasing in performance.

VI. CONCLUSION

Based on result, it can be concluded that strain technology is capable to improve the CMOS device performance. STI has shown better performance compared to LOCOS. Drain

current extracted from the STI module has increased up to 13.8% compared to conventional LOCOS module. This proved that STI is the best isolation module for 140nm transistor.

In addition, NMOS with Si_3N_4 capping layer has shown an improvement of 1%. However, variation of Si_3N_4 capping layer thickness does not shown any significant impact on the electrical properties. Furthermore, PMOS with silicide compressive stress improve 2.5% drain current. Overall, STI module contributes higher impact to the device performance compared to silicide and Si_3N_4 capping layer stress. Combination of STI and silicide module further increases the PMOS device performance significantly.

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