Integrated Current-Sensing Circuit with Offset-Current Cancellation for DC-DC Boost Converters using 0.13µm CMOS Technology

Intan Shazana Shamsul Sahar, Tuan Norjihan Tuan Yaakub

Abstract--- **The project proposed a configuration of CMOS current sensing circuit with offset-current cancellation for boost converters. This design will contrast the power and operational sensing speed with the traditional proposed current-sensing circuit. By eliminating the offset-current, it will improve the current sensing performance. It can be accomplish by applying current mirror as opposed of utilizing operational amplifier as a voltage follower in conventional design which serves to subside power consumption due to reducing the number of transistor. Moreover, this proposed design also can cancel off the offset-current in the traditional current sensing circuit, thus the improvement of sensing-accuracy will accomplished. The proposed design will be designed using 0.13µm technology and simulation will be carried out in Mentor graphics. The dc-dc boost converter will be set with operating frequency of 500kHz and designed with the supply voltage of 2V.**

Keyword--- current-sensing circuit, DC-DC Boost Converters, offset-current, low power consumption, sensing-accuracy

I. INTRODUCTION

These days, electronic gadgets are generally utilized as a part of our day by day life. The manufacturer has given careful consideration on the size, proficiency, low power dissipation and dependability of power converters in the portable electronic gadgets. Subsequently, usage of low power converter turns into the most imperative calculate request to design a superior power management circuit design on a single chip. CMOS transistor execution is the most ideal since it used less power and does not create as much heat as conventional Bipolar Junction Transistor (BJT) which may drive the circuit faster. As respects, current-sensing circuit application for DC-DC boost converter of low power and smaller chip-size is the critical thought to be highlighted.

There are various current-sensing techniques that had been produced to sense the inductor current. Nonetheless, each of these strategies has its own constraint. One of the methods is by adding a sense resistor in series with the inductor [15]. By this strategy, the issue will influence the effectiveness degradation of the DC-DC converters where the sense resistor will suffer over power loss. Another technique is current-sensing transformer technique [10] which has significant snag of high cost and larger size. Moreover, this strategy is not proper since transformer cannot exchange the DC bit of current for over-current protection. Normally, current-sensing circuit for current-mode boost converters is actualized by operational amplifier with a specific end goal to propose basic sensing circuit and functions well with low voltage supply [16]. In any case, the circuit design has fundamental disadvantages which rely on upon the operational amplifier itself. This is on the grounds that; it may influence the sensing speed because of the noise issue which the most predominant in circuit working under low signal condition.

Thereby, this research intends to design an integrated current-sensing with offset-current cancellation for DC-DC boost converter with a standard 0.13µm CMOS technology. The current-sensing circuit has great change on its power with less transistor count and offer higher sensing speed. Also, this current sensing circuit proposed without operational amplifier which will exterminate the undesirable issues, for example, additional die area, cost and high power consumption. Therefore, this proposed current-sensing circuit will be helpful for versatile DC-DC converters particularly in power electronic application.

II. DESIGN ISSUES OF DC-DC BOOST CONVERTER

A. DC- DC Boost Converter

The primary purpose of the DC-DC boost converter is to senses the inductor current for over-current (over-load) protection, paying little mind to the sort of feedback control [5]. There are two types of DC-DC converter which is boost and buck converter. Both of these types of converter have its own functions and limitations. For the DC-DC converter that can step output voltage up higher than input is boost converter, buck converter will invert the input voltage and step output voltage down than input. Also for step up and down is called buck-boost converter that is simultaneously through the linear regulator simply can make output voltage lower than input voltage [9]. Therefore, it demonstrates that the DC-DC converter is so useful to the many portable applications. In order to enhance the effectiveness characteristic of the converter, the power loses should be minimized [9].

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The DC-DC boost converter with current sensing technique is executed to integrated circuit where a typical example of an integrated circuit (IC) boost converter such as LM27313 from Texas Instruments. This chip is intended for use in low power systems, for example, PDAs, cameras, mobile phones, and GPS devices. As for understanding, the fundamental structure of boost converter is demonstrated in Fig. 1. At the point when the switch S_{ON} is on, the current that is proportional to the battery voltage is preserved at external inductor. At the point when the switch S_{OFF} is on, the preserved voltage is used to charge the output capacitor for regulation. At the static state, output voltage is acquired as the proportion of T/TOFF because the amounts of current at each phase are the same [9].

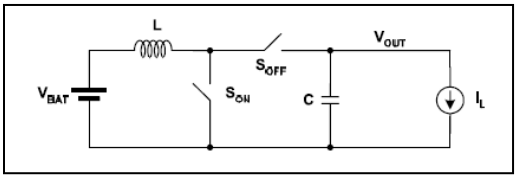


Figure 1. Basic formation of DC-DC Boost Converter

B. Current-Sensing Circuit

Current-sensing is a method of determining the current drawn to a load. Concurrently, current-sensing or current-mode signaling decides the logic value transmitted on a wire based on the current through the wire. This is in direct difference to voltage-mode [11] which characterizes logic levels as voltages on the output nodes [1]. The most basic technique for sensing the output current of current-mode converters [6,13] is to use a sensing resistor in series with the inductor or power transistor. The primary concern of this methodology is its high power dissipation as all the inductor current or drain current of the power transistor must pass through the sensing resistor [4].

a) Conventional Current-sensing design

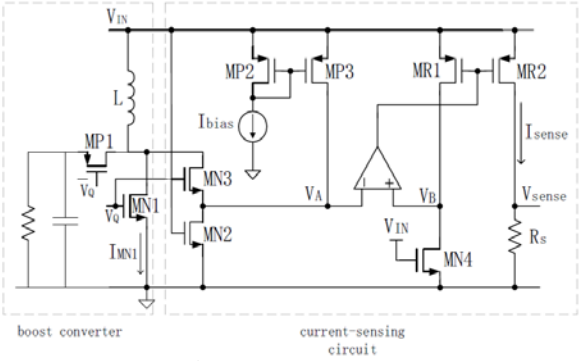


Figure 2. Schematic of Conventional Current-Sensing Circuit [15]

Fig. 2 shows the schematic of conventional current-sensing circuit for boost converter. Xuehui Tao *et al.* [15] proposed the conventional integrated current-sensing for current mode control converter that designed with 0.6 µm CMOS technology for boost converter. The proposed sensing circuit was straightforward and function admirably with low voltage supply. Nonetheless, the proposed circuit design has main disadvantages which rely on upon operation op-amplifier that will prompt undesirable issues, for example, extra cost [16] which in the meantime the packaging cost as well goes high [7]. Moreover, since the proposed circuit design is execute the op-amplifier, it may influence the sensing speed because of the noise. The noise issue is most predominant in circuit working under low signal condition.

This type of current-sensing circuit offer with low voltage supply [12] which indirectly will improve the power saving. The primary concern of this sensing scheme is the precise value of Rs that is needed for control of the converters. If Rs is small, the sensing signal is not sufficient enough to control purposes and an additional operational amplifier (op-amp) or current-sensing amplifier is needed. However, if Rs is large, its high power dissipation decreases overall efficiency [17] of the converters, especially for low-voltage high-current applications. In addition, Rs varies with temperature and different procedures and hence influences accuracy [4].

b) Proposed Current-sensing design

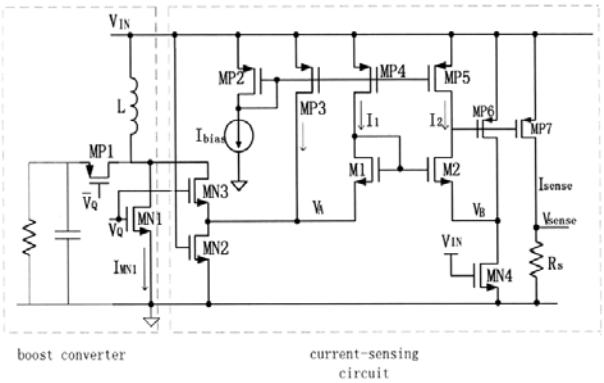


Figure 3. Schematic of proposed Current Sensing Circuit [16]

Proposed circuit design descriptions: Fig. 3 shows the proposed current sensing circuit [3]. A few modifications have been made by implement voltage follower to substitute the routine op-amp. The voltage follower function as to make the voltage VA=VB, while the drain current of transistor MN2 is mirrored to transistor MN4 that is

$$I_{MN4} = I_{MN2} = \frac{I_{MN1}}{2N} + I_{bias} \quad (1)$$

As for the current of transistor MP6 is;

$$I_{MN6} = I_{MN4} - I_{M2} = \frac{I_{MN1}}{2N} + I_{bias} - I_{bias} = \frac{I_{MN1}}{2N} \quad (2)$$

The modification of current-sensing technique using a current mirror is done in order to overcome power loss to the circuit. As the sensed inductor current is scaled down, the power loss in the sensing circuit will perceptibly lower. Furthermore, the accuracy of the sensed inductor current also depend on the current mirror of the circuit with the resistor, Rs [5]. As for the sensing resistor, Rs, the resistance must be in a small value as to reduce the power loss [14]. This is because, when the power is turn on, the current flow through the resistor, the cross voltage sense is proportional to the sensing current. For the current Isense, that flowing through the resistor, Rs is the scaled of inductor current which as stated in (3) that is exactly proportional to and much smaller than the inductor current.

$$I_{sense} \ll I_L = \frac{I_{MN1}}{2N} \quad (3)$$

The difference in the proposed offset-cancellation scheme is that a summing amplifier is utilized to program and cancel the offset. The aim of selecting this design is that to reduces clock feed-through and charge injection, consequently improving offset cancellation performance, all without adversely influencing bandwidth [8].

III. DESIGN METHODOLOGY

Flow chart in Fig. 4 shows the step to design the high sensing speed and low power of proposed Current-sensing for DC-DC Boost Converter.

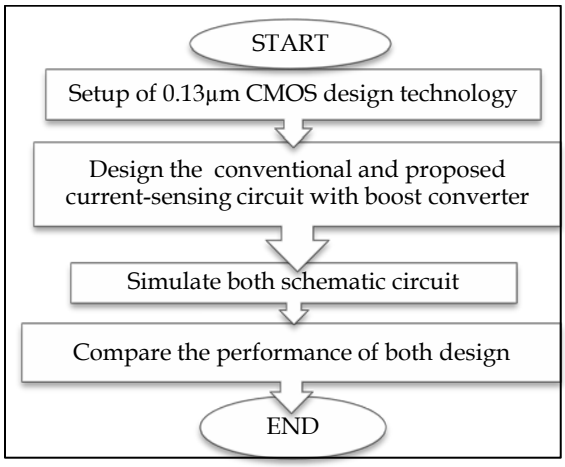
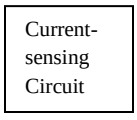


Figure 4. The design and simulation flow chart

The schematic simulated by the Design Architecture tool. The design is then will be check whether there is an error that need to troubleshoot. Then, both schematic will analyze based on the performance of each circuit design. If the results meet as expected, the design will proceed with layout design. As result, the waveform generated will be analyzed and observed based on theory and also as the specification meet the objective.



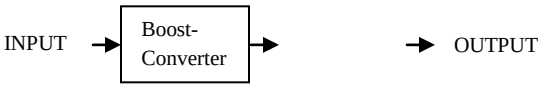


Figure 5. Block diagram of DC-DC boost converters and current sensing

The designs carry out to investigate the better performance of current-sensing design for boost converter in terms of power and sensing accuracy. The proposed circuit design current mirror instead of using operational amplifier as a voltage follower which would reduce power consumption. This design also adds cancellation of the offset-current for better sensing-accuracy compared to the conventional current sensing circuit. This design will carry out in schematic and layout using the 0.13 µm CMOS technology from Mentor Graphic Software.

IV. RESULT AND DISCUSSION

This section provides the comparison performance of both current-sensing designs has been analyzed using Mentor graphic by using 0.13µm CMOS technology for conventional current-sensing and proposed current-sensing circuit design. After the simulation for both design are made, the performance of sensing-accuracy and power are observed and recorded. The simulation for both designs has been done by considering the supply voltage of 2V with frequency of 500kHz. The bias current, I_{bias} of 3µA and sensing resistor, R_s to be 400Ω used for current –sensing operation which is 2.0V.

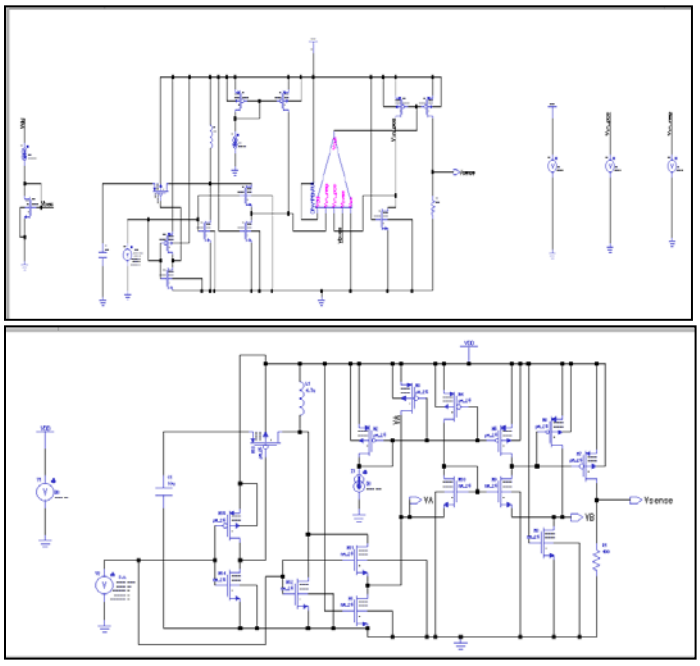


Figure 6. The schematics of conventional (upper graph) and proposed current-sensing circuit (bottom graph) of current-sensing circuit

Fig. 6 shows the schematics of conventional and proposed current-sensing circuit. The difference between both designs

was the presences of the operational amplifier for the conventional design. As shown, the proposed design offers less transistors compared to recently propose. Then, the results observed in term of its sensing accuracy, power dissipation and also power consumption. All of the results are shown below.

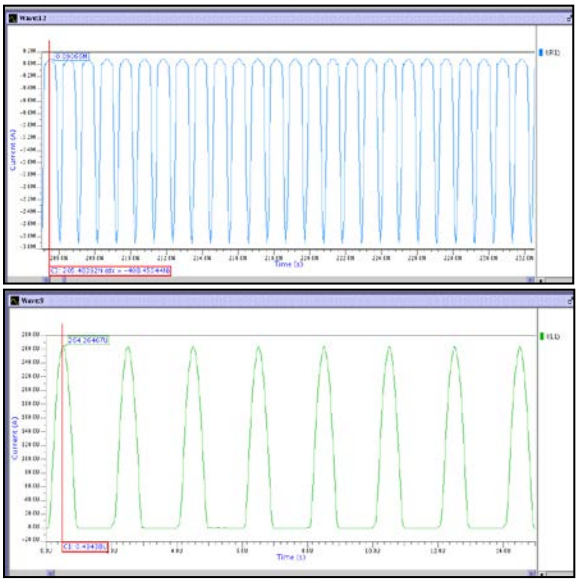


Figure 7. The simulation results of current sensing signal (upper graph) and inductor current (bottom graph) for conventional current-sensing circuit

Fig. 7 shows the simulation results of conventional current-sensing circuit of current sensing signal at 0.09066mA with inductor current at 264.26467µA.

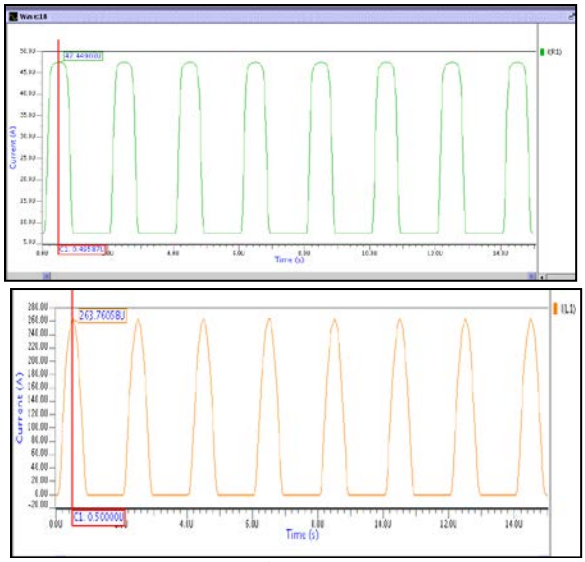


Figure 8. The simulation results of current sensing signal (upper graph) and inductor current (bottom graph) for proposed current-sensing circuit

Fig. 8 shows the simulation results of proposed current-sensing circuit of current sensing signal at 0.047451mA with inductor current at 263.76058µA.

TABLE I. COMPARISON OF INDUCTOR AND SENSING CURRENT FOR BOTH CURRENT-SENSING DESIGN

Current-sensing. Design	Inductor Current, I_L (µA)	Sensing Current, Isense (mA)
Conventional Current-sensing Circuit	264.26467	0.09066
Proposed Current-sensing Circuit	263.76058	0.04745

Table I shows the comparison of inductor and sensing current between conventional and proposed current-sensing design. Both designs have operated well as the sensing current generates lower than the inductor current theoretically. Furthermore, as can be seen from Fig. 7 and Fig. 8 that the proposed sensing circuit is able to sense the rising slope of the inductor current accurately. Indicates that the values of the inductor and sensing current for proposed current-sensing circuit is slightly lower than the conventional current-sensing. This shows that the proposed current-sensing circuits works well since new current-sensing parts have been modify without using the operational amplifier. Therefore, the high sensing can be achieved as the performance in terms of power and transistor count of the current-sensing circuit also discussed below:

TABLE II. PERFORMANCE OF CURRENT-SENSING CIRCUIT

Current-sensing. Design	Power Consumption (mW)	Power Dissipation (µW)
Conventional Current-sensing Circuit	724.65596	372.7695
Proposed Current-sensing Circuit	0.74145	51.0481

A. Power consumption

Power consumption is defined as:

$$P = I_{DD} \cdot V_{DD} \quad (4)$$

Typically, CMOS technology has been praised for its low static power. During switching in CMOS for a short period, NMOS and PMOS are simultaneously active and the instantaneous short-circuit current flows from the power supply direct to ground [2]. Thus, the total short circuit current will subscribe for the power consumption.

Based on the results obtained, the result of the power consumption was slightly difference. Theoretically, the lower the power consumption, the better the performance would be. Thus, based on Table II, the proposed current-sensing circuit have low power consumption compared to conventional design. This shows that the proposed current-sensing design offered better performance and high sensing speed.

B. Power dissipation

Table II notify the power dissipate for both current-sensing design. In mentor graphics, the power dissipation value is then obtained by using the result browser after the simulation is completed. Based on the power dissipation results, found that the proposed current-sensing design have produced low power dissipate compared to the conventional design. This is clearly because of the large transistor count and the arrangement of transistor that the conventional current-sensing designs have. Since to that, the power dissipation will increase and indirectly will reduce the performance of the sensing circuit. Furthermore, since the manufacturer has given much attention on low power dissipation of power converters, thus the proposed current-sensing design have fulfilled one of the industry demands.

C. Transistor count

Based on the results obtained, there are differences of power between both current-sensing designs. This is due to both of current-sensing design used the different number of transistor count. The transistor count can be reduced by making modification to the existing configuration in order to improve the efficiency. As for this proposed design, the number of transistor count have been modify compared to the conventional design that need more transistor for the operational amplifier. Thus, it will offer higher current-sensing accuracy than the existing current-sensing circuit. Less transistor means there will be less power consume by the circuit which will increase the performance of the circuit. Since the transistor count reduce, the complexity of the circuit also deductible compared to the conventional design of current sensing.

V. CONCLUSION

This paper has presented a precise CMOS current-sensing circuit for boost power converter. The simulation results of better performance of sensing-accuracy and low power dissipations using 2V power supply are presented. The comparison between the conventional and proposed current-sensing circuit also included. Since the new current-sensing circuit does not use op amplifier, low power and high sensing-accuracy achieved.

In conclusion, the proposed design shows the improvement on sensing-accuracy, speed and also minimization both power consumption and dissipation of the current-sensing circuit design since a better implementation has been taken. Thus, the proposed current-sensing design offer higher current-sensing accuracy compared to the conventional design. Besides, this proposed design has reduced the complexity of the design; therefore it may decrease the cost greatly. Indirectly, this current-sensing circuit will be benefit in portable DC-DC converters applications.

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