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Low-Power Current-Mode Resistive Readout Circuit Using 0.13µm Technology for biomedical MEMS applications

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***Abstract*— This paper presents an innovative current-mode interface circuit design specifically for resistive readout circuits. The main goal is to create and evaluate resistive readout circuits utilizing a current-mode architecture. The design and simulation of the resistive readout circuit are conducted using Silterra's 0.13µm technology, powered by a 1.2V supply voltage, with the aid of Cadence ADE. This architecture is optimized for low power consumption, drawing only 15µW, while maintaining high sensitivity for resistive values ranging from 500KΩ to 199MΩ. The circuit's output voltage varies between 0.48V and 1.03V, allowing for precise measurement and analysis of resistive sensor data.**

***Index Terms*—Interface circuit, Mems resistive sensor, Readout circuit,Resistive sensor circuitry.**

I. INTRODUCTION

Biomedical Microelectromechanical Systems (Bio-MEMS) sensors are revolutionizing the healthcare industry by offering innovative solutions for diagnostics, monitoring, and treatment applications. These miniaturized devices integrate mechanical and electrical components at the microscale, enabling precise detection and measurement of various physiological parameters [1]. Their primary applications include monitoring vital signs, detecting diseases, managing chronic conditions, and enhancing drug delivery systems. Biomedical MEMS sensors are invaluable in patient care and medical research with their high sensitivity, accuracy, and non-invasive operation.

The significance of biomedical MEMS sensors lies in their ability to provide real-time data, facilitate early diagnosis, and improve patient outcomes. Their small size and low power consumption allow integration into portable and wearable devices, enhancing patient mobility and comfort [2]. Furthermore, advancements in MEMS technology continue to drive innovation in medical devices, contributing to more personalized and efficient healthcare solutions. MEMS sensors have garnered tremendous attention in the medical field due to their capability to adapt to environmental conditions, acquire data, and translate them into electrical signals, making them ideal instruments for medical applications [3], [4], [5].

Among the various types of biomedical MEMS sensors, resistive sensors serve as a promising platform for monitoring human physical conditions. Research conducted by the Department of Physics at the University of Illinois at Urbana-Champaign has revealed that human body resistance can vary significantly from one individual to another [3]. Additionally, the resistance of different body parts can vary due to differences in skin thickness and the epidermis layer beneath the skin [3]. Notably, the resistance of dry skin can range from 300Ω to 1,000Ω, according to the findings [3]. These insights highlight the potential of MEMS resistive sensors in providing valuable data for personalized health monitoring and diagnosis.

Collateral with the development of the MEMS resistive sensor, the establishment of constructing the readout circuitry for the sensor has never ended. Various designs of circuits have been proposed and studied by designers and researchers to accomplish a low power design. To obtain high sensitivity, large voltage supply to Wheatstone bridge and small resistance changes are preferred [6] and bridge-output-to-frequency conversion is dominant because of circuit simplicity and high linearity [7]. The circuit design for wide input resistance range is challenging [8], [9] and [10]. The architecture in [11] represents the most effective wide-range resistance. Hence, this paper will explain thoroughly the proposed design to realize a low-power design.

This paper is organized into four main sections: Section II examines previous research on the design of low-power readout circuits; Section III outlines the proposed methodology in line with the paper's objectives; Section IV presents the simulation results of the designed circuit; and Section V provides the conclusions of the study

II. LITERATURE REVIEW

A variety of designs have been developed by researchers to create low-power resistive sensor readout circuits. This section provides an overview of previous studies, analyzing the concepts and methodologies employed by researchers in their circuit constructions. These innovative designs are focused on improving the efficiency and accuracy of resistive sensor readout circuits, addressing the increasing need for energy-efficient sensor technologies.

The development of a MEMS gas sensor interface circuit utilizing SAR ADC technology is described in [12]. The circuit incorporates a sensor resistor array, a multiplexer, a pre-amplification stage with an operational amplifier, a low-pass filter, a SAR ADC, and a digital signal processing unit. The pre-

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stage circuit uses a Wheatstone bridge, a low-noise chopping operational amplifier with variable gain, and a 4th-order active low-pass filter. The 12-bit SAR ADC uses a hybrid capacitor-resistor (C-R) DAC structure with additional multiplexer, boost, and buck circuits to optimize power consumption. The conversion error is within 0.5-1% for sensor resistances from 100 Ω to 1 MΩ. The total power consumption is 986 μW with a 3.3 V supply voltage.

A novel ultra-low-power read-out circuit for interfacing gas sensor matrices is presented in [13], targeting applications in gas sensing for Internet of Things (IoT) devices. The circuit is designed to overcome the challenges associated with interfacing different types of gas sensors. The circuit utilizes a relaxation oscillator architecture, which is known for its ability to handle large dynamic ranges. The design features a voltage reference circuit, current mirrors, an integrating capacitor, comparators, and a set-reset (SR) register to produce a triangular waveform, where the period corresponds to the sensor's resistance. Fabricated using a 180 nm bulk CMOS process, the circuit was tested, proving its capability to interface with sensors over a broad resistance range from 1 kΩ to 33 MΩ. It generates a bias voltage ranging from 50 mV to 1 V, optimizing sensor performance. The circuit operates with minimal power consumption, with a maximum current draw of 194 μA.

The proposed circuit in [14] is a fully integrated CMOS-MEMS bidirectional flow sensor with low power pulse operation. The paper highlights that previous integrated flow sensors either suffered from limited sensitivity, large area, high power consumption, or unidirectional sensing capabilities. The proposed circuit offer high sensitivity, low power usage, a compact design, and bidirectional sensing capabilities. It combines a thermoresistive micro-calorimetric flow (TMCF) sensor, manufactured on a MEMS wafer, with a low-noise instrumentation amplifier integrated on a CMOS wafer.. The TMCF sensor is arranged in a Wheatstone bridge configuration. The instrumentation amplifier, utilizing a current feedback instrumentation amplifier (CFIA) configuration, enhances the weak signal from the Wheatstone bridge and delivers a processed output. The sensor exhibits a sensitivity of 98 mV/sccm while consuming less than 9 mW of power.

The author in [15] proposes a novel low-power front-end circuit for resistive sensors based on a switch-capacitor technique with current reuse. This approach aims to address the high power consumption issue common in traditional resistive sensor readout circuits like voltage dividers and Wheatstone bridges. The circuit is designed primarily for differential resistive sensors, where two sensors (Rs1 and Rs2) change their resistance in opposite directions. This configuration allows for efficient current reuse and power reduction . The result shows the power consumed for three different resistance values of 0, 2.5kΩ and 5kΩ are 120μW, 225μW and 420μW respectively. The proposed circuit offers a promising solution for reducing power consumption in resistive sensor applications. However, the circuit's performance is inherently limited by the charging and discharging time of the capacitor (Cs). This limits the bandwidth and makes it unsuitable for applications requiring fast response times or high-frequency measurements

While [16] has proposed a digital interface circuit for resistive sensors, called the Digital Circuit for Resistive-sensors (DCR). The DCR consists of two main sections:- i. Auxiliary section: This section includes an operational amplifier and the resistive sensor elements. It provides a single reference voltage, enables excitation current control, and allows for high-current excitation of SE sensors, and ii. Dual-slope section: this section comprises a switch, an integrator, a comparator, and a Timing and Logic Unit (TLU). It performs the dual-slope conversion process, measuring the time durations to determine the sensor resistance. The circuit exhibits very low nonlinearity, with a maximum experimental nonlinearity of 0.06% observed across various sensor configurations which indicates high accuracy in resistance measurements. The DCR can interface with various types of resistive sensors, including single-element (SE), differential (DS), half-bridge (HB), and full-bridge (FB) configurations. However, the dual-slope architecture inherently limits the bandwidth of the circuit, making it unsuitable for applications requiring high-speed measurements. Furthermore, the proposed work uses a discrete circuit with 10V supply not suitable for low power design solution.

In this paper [17], the authors present a comprehensive design and analysis of a resistive sensor interface, which includes three distinct designs that enable scalability of phase noise, energy, and resolution in time-based resistance-to-digital converters (RDCs). These RDCs are characterized by a three-stage differential ring oscillator, which is current-starved by the resistive sensor, as well as a differential-to-single-ended amplifier, digital modules, and a serial interface. The baseline design of the RDC focuses on achieving low energy consumption and efficient conversion steps, forming the core of the time-based RDC structure. The second design (higher-resolution) enhances the oscillator's rms jitter and phase noise using speed-up latches, resulting in greater bit-resolution. The third design (process portability) reduces power usage by leveraging improved phase-noise design and technology scaling, achieving a 1-bit resolution improvement over the second design. The RDCs offer scalable energy and resolution capabilities. Design 1 operates at 861 nW with an 18-bit resolution using TSMC 0.35 μm technology, featuring a 10 ms read-time and a single readout per second. Designs 2 and 3, both with a 10 ms read-time and repeated once every second, consume 19.2 μW and 17.6 μW, respectively, and offer a 20-bit resolution with TSMC 0.35 μm and 0.18 μm technologies. Remarkably, Design 3 achieves a 21-bit resolution with a 30 ms read-time, marking the highest resolution recorded for a time-based ADC. The 0.35-μm RDC design stands out for its minimal power consumption among time-based ADCs, whereas the 0.18-μm RDC, enhanced with a speed-up latch, achieves superior resolution. All designs maintain an active chip area below 1.1 mm^2. This time-based RDC design presents an attractive solution for applications requiring low-power and high-resolution sensing, particularly in scenarios where the input signal is slow and the measurement time is less critical.. However, its limitations in bandwidth and jitter sensitivity need to be carefully considered for specific applications.

The [18] proposes two novel Direct Interface Circuits (DICs) for simplifying the readout of resistive sensors. Both circuits utilize only passive components (capacitors and resistors) and a Digital Processor (DP). The DICs estimate the sensor resistance (Rx) using a single charging-discharging process. The proposed circuits eliminate the dependency on the output resistance of the DP pins, leading to improved accuracy in Rx estimation. The single charging-discharging process and the absence of calibration steps contribute to reduced energy consumption. The two proposed DICs are i. Two-Capacitor Interface (TCI). This circuit uses two capacitors (CA and CB) and the sensor (Rx) to determine Rx based on the time difference (△T) between the discharge times of the two capacitors and ii.Single-Capacitor Interface (SCI).: This circuit employs a single capacitor (C) and the sensor (Rx) to estimate Rx using the time difference (△T) between the discharge times of the capacitor and a known resistor. The experimental results demonstrate that the proposed TCI and SCI circuits consume 178µW-396.7µW and 315µW-721µW respectively for 221 Ω − 24.9 kΩ range of resistance. The proposed DIC solutions offer significant advantages in terms of simplicity, speed, and energy efficiency. However, their accuracy might be limited for extreme resistance values, and they are sensitive to variations in capacitor values.

This literature review examines seven papers presenting various approaches for interfacing resistive sensors with digital systems, focusing on low power consumption, high accuracy, and wide dynamic range. Papers [13], [17], and [18] demonstrate the lowest power consumption, making them suitable for battery-powered IoT applications. Papers [12] and [16] achieve the highest accuracy, suitable for precision measurements. Papers [13], [17], and [18] offer the widest range of sensor resistance compatibility. Papers [12], [14], and [15] are more suitable for applications requiring faster response times.. Each approach involves trade-offs among power consumption, accuracy, bandwidth, and dynamic range. Given that this work focuses on designing resistive sensor readout circuits for biomedical applications, where battery life and accuracy are crucial, FETs-based read-out circuitry emerges as the optimal solution.

III. METHODOLOGY

There are two types of Wheatstone: current mode Wheatstone bridge [19] and Voltage-driven Wheatstone bridge. The Voltage Driven Wheatstone Bridge structured by having one, two or four sensor resistors and one of example two elements varying which values deviate with the physical variable as shown in Fig.1. The important characteristics of the resistive sensor are sensitivity and wide bandwidth [3] and [4]. To increase the sensitivity of the resistive sensor, the bridge should be balanced among resistors and the requirement is very difficult to achieve in a two-element varying Wheatstone Bridge in this architecture with a larger physical layout area and the range of resistive value depends on the maximum of the balanced resistors R_1 and R_2 since need to tune ΔR in R_0± ΔR. The main challenge with the voltage-driven Wheatstone bridge lies in its sensitivity, S which is directly proportional to the supply voltage, V_{DD} and and inversely proportional to the sensor resistance as in (1). To enhance sensitivity, a higher V_{DD} and a sensor with a very low resistance are needed, leading to increased power consumption.

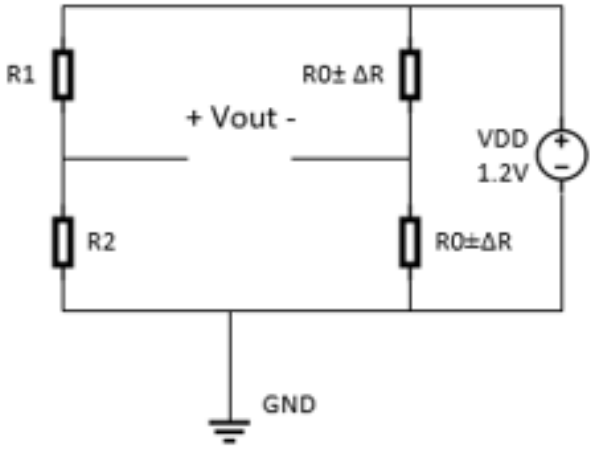

Fig.1. Conventional Voltage-Mode Wheatstone Bridge

$$S = \frac{V_{out}}{\frac{\Delta R}{R_0}} \tag{1}$$

Where

$$V_{out} = (V_{out2} - V_{out1}) \tag{2}$$

$$V_{out1} = \frac{V_{DD}(R_0 + \Delta R)}{((R_0 + \Delta R) + (R_0 - \Delta R)} \tag{3}$$

$$V_{out2} = \frac{V_{DD}(R_1)}{((R_1) + (R_2)} \tag{4}$$

The current-mode Wheatstone Bridge has been introduced which based on circuit duality concept [20]. The dual network Wheatstone Bridge is straightforward concept of differentiation of current, ΔI as in (5) which is proportional of the changes in resistance. Current-mode Wheatstone Bridge inherits the characteristic of Voltage-mode Wheatstone Bridge in term of stability, sensitivity and linearity since it is circuit duality.

$$\Delta I = I_2 - I_1 \tag{5}$$

This paper proposes a new architecture of current mode arrangement that suitable for low-voltage application. The architecture shown as in Fig.2 (circuit level) and Fig.3 (transistor level) uses two of resistors connected between excitation voltage, V_B and an input voltage, V_1 of current mode amplifier. Under the variation resistive sensor, the ΔIcurrent will change accordingly. There are two output conditions, high state and low state. The high state give maximum resistive output while the low state is dedicated for the minimum

resistive output. The notation for high state are R_{2H} and R_{1H} and the low state notation are R_{2L} and R_{1L} . The novelty of this architecture allowed designer to define the ΔR for resistive sensor readout circuit. The condition of high state is when $R_{2H} \gg R_{1H}$ and $R_{2H} \gg R_{2L}$ with $R_{1H} \ll R_{1L}$ and R_1 and R_2as (6) and (7) respectively and the minimum output resistive output occurs when $R_{2L} \gg R_{1L}$. The change current, ΔI is proportional of the ratio on ΔR_H for high state or ΔR_L for low state with R_0 and proportional to the multiplier of the differences of V_B and V_1 as in (12).

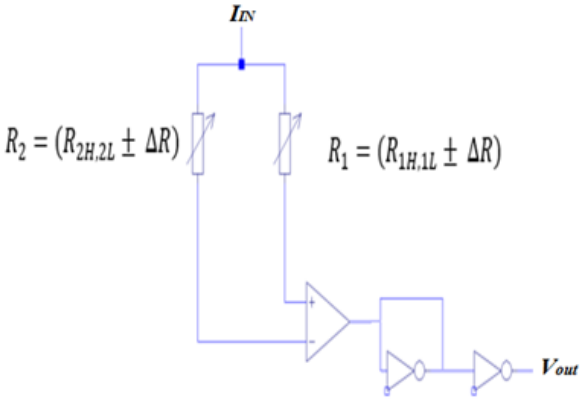

Fig.2. Resistive Sensor Readout Circuit (Circuit Level)

$$R_1 = (R_{1H,1L} \pm \Delta R) \quad (6)$$

$$R_2 = (R_{2H,2L} \pm \Delta R) \quad (7)$$

Where

$$\Delta R_{state} = R_{2H} \pm R_{2L} = R_{1L} \mp R_{1H} \quad (8)$$

$$\Delta R_{range} = R_{2H} + R_{1H} = R_{2L} + R_{1L} \quad (9)$$

$$\Delta R_H = R_{2H} - R_{1H} \quad (10)$$

$$\Delta R_L = R_{2L} - R_{1L} \quad (11)$$

Therefore

$$\Delta I = \left(\frac{2(V_B - V_1)}{R_{1H,1L}}\right)\left(\frac{\Delta R_{H,L}}{R_0}\right) \quad (12)$$

The Current-to-Voltage converter as in Fig.4 is one of vital block in Resistive Sensor Readout architecture. This architecture suitable for wide range of current to voltage conversion without using capacitor for charge accumulation process. The input current for this circuit can either positive or negative and for this design, the size of NMOS and PMOS are identical. The changing of the current related to transistor operation.

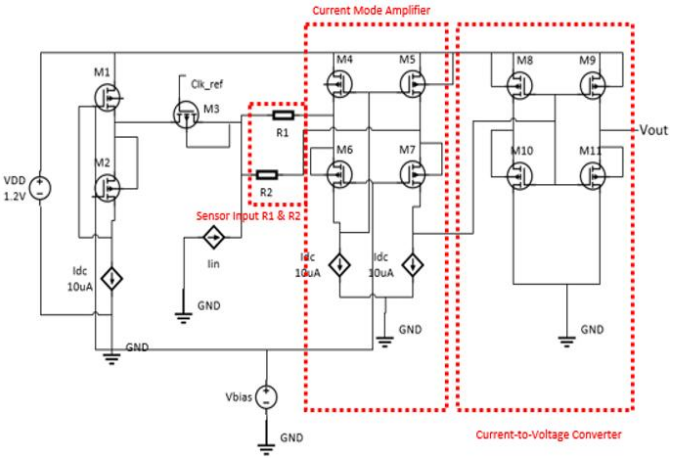

Fig.3. Resistive Sensor Readout Circuit (Transistor Level)

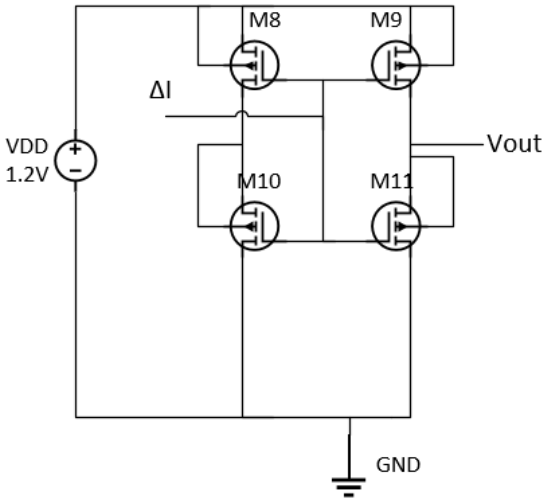

Fig.4. Current-to-voltage converter

There are three level of current input condition such as weak current (13), medium current (14) and strong current (15) and (16). When the current input ΔI in pico ampere, this consider as weak current input the variation of NMOS and PMOS transistors are small. The voltage output is related to internal resistance of PM1 and NM1.

If the ΔI in nano to micro ampere, this consider as medium current and the transistor operates within either saturation or linear region and it is continuous function of Vds related to function of input signal ΔI.

If the ΔI in strong current (micro range), the voltage variation for transistors will be more significant. If ΔI is more than zero, PM1 will operate in linear while NM1 will operate in saturation then the output voltage, Vout will depend on input current and internal resistance of PM1. If ΔI is less than zero, the output voltage will depend on the input current and proportional to internal resistance of NM1.

When ΔI in weak (pA)

$$V_{out} = \Delta I(\frac{rPM1}{rNM1}) \quad (13)$$

When ΔI in medium (nA-µA)

$$V_{out} = \frac{\Delta V_{ds}}{\Delta I_{ds}} \quad (14)$$

When ΔI in strong (µA)

$$V_{out} = \Delta I(rPM1) \quad (15)$$

$$V_{out} = \Delta I(-rNM1) \quad (16)$$

IV. Result and Discussions

The resistance to current conversion circuit presented in Fig.3.The circuit was designed and simulated using the 0.13µm CMOS process supplied by Silterra.The supply voltage , V_DD was set to 1.2V and the bias current is I_dc = 10µA.The design has been simulated using ADE Cadence Transient response.Transistor dimensions shown as in Table 1. The simulation of current-to-voltage converter as shown in Fig.5. The resistance limit of R_1 and R_2 versus the output voltage is shows in Fig.6. The Fig.7 is the simulation results from parametric analysis by varying maximum and minimum of R_1 and R_2. Fig.8 shows the transient response for Voltage Mode Wheatstone Bridge with two-element varying. The clock is controlling the output resistive with difference $R_2 - R_1 = \Delta R$ which $R_2 = 3.147M\Omega$ and $R_1 = 1K\Omega$ respectively. The simulation output for proposed current mode circuit are shown as in Fig.9 and Fig.10 with different resistive sensor inputs. The pass transistor M3 act as clock timings controlling the output resistive. The differences of resistive sensor ΔR in high state between R_{2H} and $R_{1H}$is 199 MΩ with the output voltage V_{out} is 1.03V as shown in Fig.9. The difference of resistive sensor ΔRin low state between sensor R_{2L} and R_{1L} by 4MΩ with the output voltage of 0.48V as shown in Fig 10. From the transient response results, the proposed current-mode sensing architecture gives flexibilityfor the user to define the resistive range in high state and low state which is ΔR_{state} and ΔR_{range}. The proposed current mode circuit has high resistive range compared to Voltage-mode Wheatstone Bridge.

TABLE I. Resistive Circuit Parameters

Transistor	Size(W/L µm)
M1, M4,M5	11/1
M2, M6, M7	50/1
M8, M9	3/20
M10, M11	1/2
M3	32/1

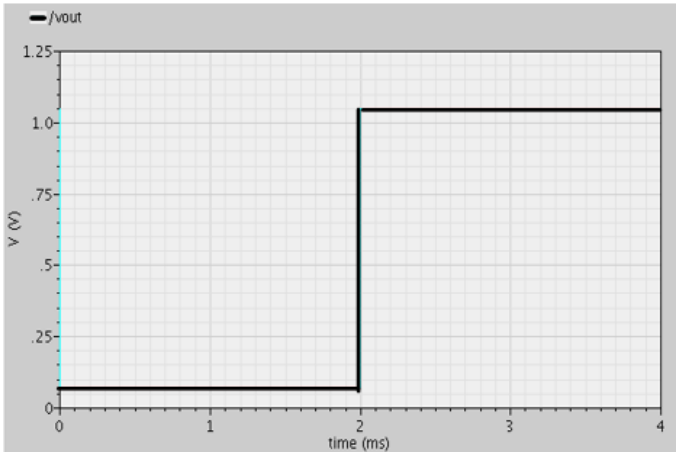

Fig.5. Output Current-to-Voltage converter from 1pA to 1mA

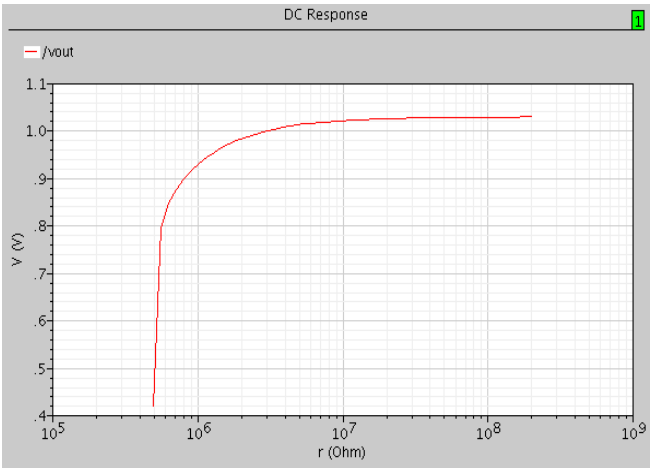

Fig.6. Simulation of resistance limit reflect to output voltage

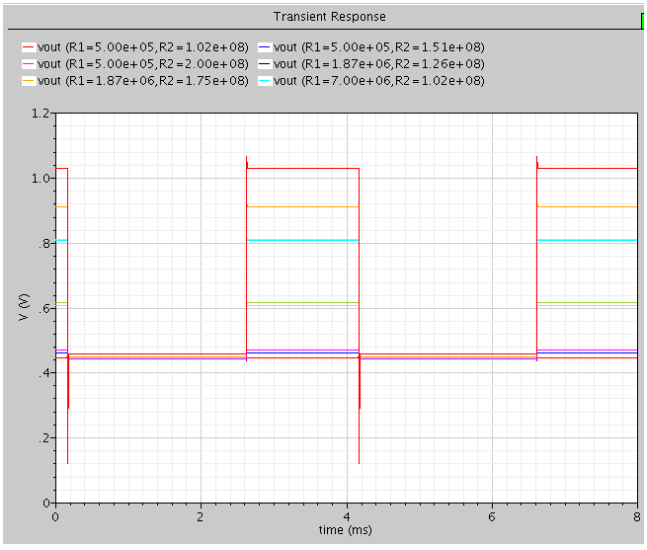

Fig.7. Parametric Analysis by varying R1 and R2 sensors input

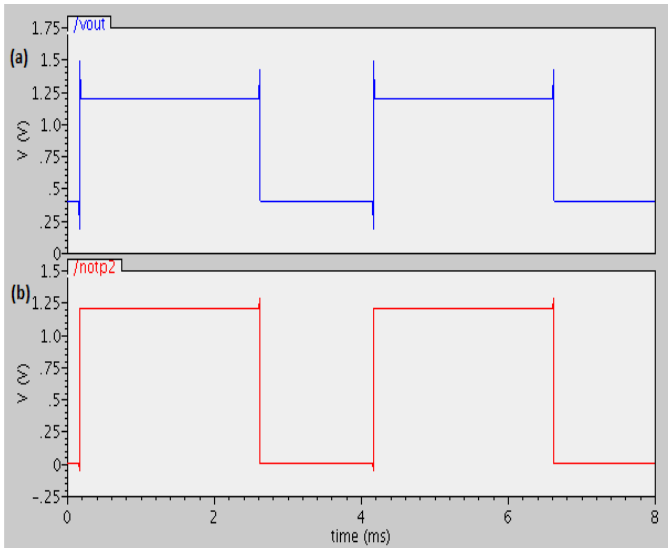

Fig.8. Voltage-mode Wheatstone Bridge: (a) Output voltage when Δ R = 3.469MΩ (b) Clock Input Signal

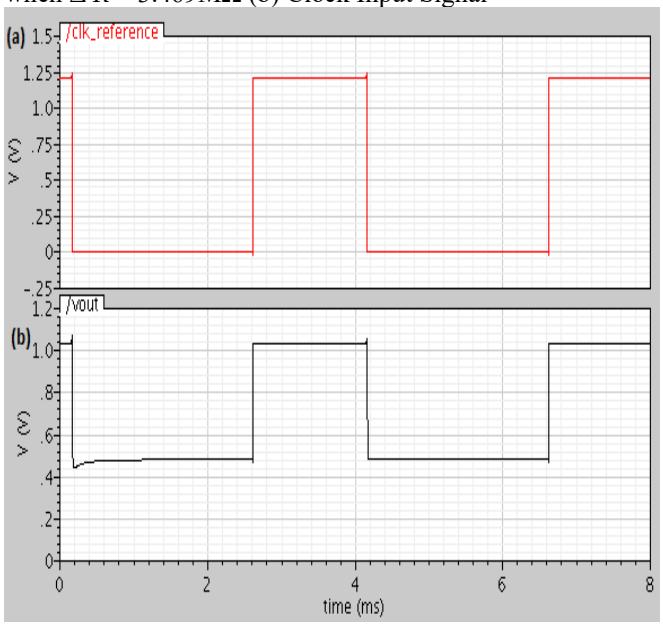

Fig.9. Current-mode: (b) Clock Input Signal (a) Output voltage when Δ R = 199MΩ in high state

Table 2 shows the performance comparison of various methods for resistive readout circuits and the proposed architecture gives better sensitivity and low power consumption.

In addition to the performance comparison presented in Table 2, further advancements in readout circuits have been made. Notably, some of these circuits demonstrate remarkably low power consumption, with figures as low as 9.75 µW [24] and 17 µW [25]. However, their maximum resistance measurement range is limited to 1MΩ [24]. Meanwhile, readout circuit systems in [26], [27] and [28] exhibit power consumption of 0.5 mW, 0.93mW and 36.3 mW respectively. The maximum resistance stated in [26] and [28] is 120kΩ and 1MΩ respectively. This analysis indicates that this work remains competitive when compared to recent achievements in the field, maintaining a balance between power efficiency and measurement capability.

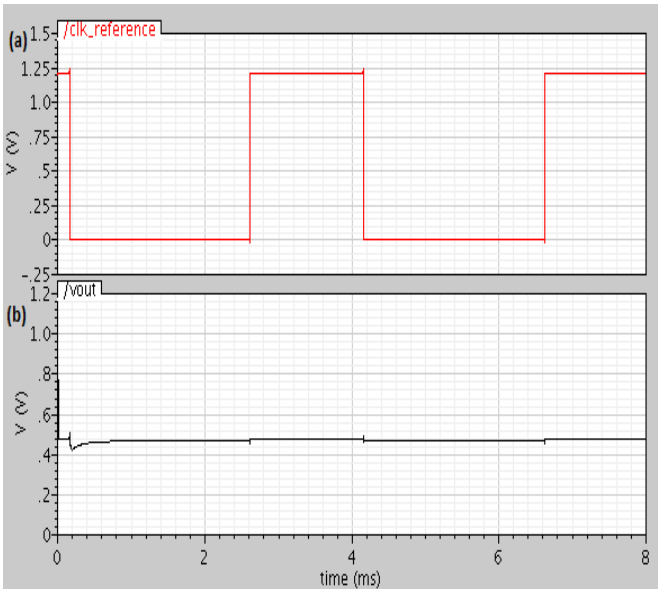

Fig.10. Current-mode: (a) Output voltage when Δ R = 4MΩ (b) Clock Input Signal

TABLE II. COMPARISON PERFORMANCE OF CURRENT MODE RESISTIVE READOUT CIRCUITS

Characteristic	Reference			
	[21]	***[22]***	*[23]*	***This work***
Process	0.18µm	32nm (CNFETs)	0.18µm	0.13µm
Max. Resistance	30MΩ	100kΩ	4MΩ	199MΩ
Power Consumption (W)	124µ	175m	1m	34.8µ

V. CONCLUSION

This paper presents a low power and high sensitivity of resistive sensor readout circuit using the current mode methodology. The novelty of this work lies on the user define resistive range based on current mode methodology which improve the power dissipation. The overall sensor readout system achieves low power consumption of approximately 34.8 µW, with a resistive measurement range from 500 kΩ to 199 MΩ. The output voltage spans from 0.48 V to 1.03 V at a supply voltage of 1.2 V. This broad range demonstrates the readout circuit's capability to effectively measure a diverse array of resistive sensors, indicating a higher selectivity.

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